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Roll No. ..... Total No. of Pages : 2

Total No. of Questions : 09

B.Tech (IT) (Sem.–5)

PARALLEL ARCHITECTURE & COMPUTING

Subject Code : IT-309

Paper ID : [A0518]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY.**
2. **Attempt any FOUR questions from SECTION-B.**
3. **Attempt any TWO questions from SECTION-C.**

SECTION-A **(10 × 2 = 20 Marks)**

1. (a) What is Reservation Table?

(b) What approaches are used for parallelism?

(c) Define the term cache corruption in Shared Memory Parallel System.

(d) What is task migration?

(e) Write a short note on Load Sharing v/s Load Balancing.

(f) What is sequential bottleneck problem in Amdahl's Law?

(g) What is SPMD?

(h) What is the difference between array processors and vector processors?

(i) What is Systolic Array?

(j) How synchronization takes place among shared memory computers?

SECTION-B **(4 × 5 = 20 Marks)**

2. Write short note on :

(i) Mutual Exclusion between Processors.

(ii) Dynamic Priority Algorithms.

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3. What is Load balancing in distributed system? Also discuss a load balancing algorithm.

4. Discuss Deterministic models for scheduling on UMA Multiprocessors.

5. Write pseudo code for prefix-sum algorithm.

6. Explain the design components of instruction pipeline.

SECTION-C **(2 × 10 = 20 Marks)**

7. Discuss various PRAM models and compare the relative powers of various PRAM models in detail.

8. Discuss the functional structures of the Multiprocessor Architecture in detail.

9. What are the various hazards involved in pipeline? How can they be resolved ?

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