Roll No. .....

Total No. of Questions : 09] [Total No. of Pages : 02

B.Tech. (Sem. - 3rd)

DIGITAL CIRCUITS AND LOGIC DESIGN

SUBJECT CODE : CS - 205

Paper ID : [A0453]

[Note : Please fill subject code and paper ID on OMR]

Time : 03 Hours **Maximum Marks : 60**

Instruction to Candidates:

1) Section - A is **Compulsory**.
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

Section - A

Q1) *(10 × 2 = 20)*

a) Write decimal 87 in BCD code.

b) What is the full form of ASCII and where do we use it?

c) What are the advantages of ECL over other logic IC families?

d) Why do we use shottky diode in TTL?

e) What are the disadvantages of DCTL?

f) Explain with block diagram what is 8 to 1 MUX?

g) Write the full form of EEPROM, PAL, PGA and PLD.

h) Approximately how many transistors can be integrated in a VLSI chip.

i) What technique needs to be used for A/D if the input signal (analog) is changing too fast?

j) List the various A/D convertors.

Section - B

(4 × 5 = 20)

Q2) Draw the circuit of a DTL NAND gate (2-input) and explain its operation.

Q3) Draw the circuit of a 4 bit D/A (R-2R) convertor and explain how this circuit converts digital data to analog.

Q4) (a) Explain the difference between the followings :

(i) S-R flip flop and Bistable multivibrator.
(ii) Combinational and sequential circuits.
(iii) EPROM and EEPROM.

(b) What is race around condition in J-K flip flop? Discuss the techniques to avoid it.

(c) Explain what do you mean by transmission line effects?

Q5) Draw the circuit of a 4 bit ring counter with negative edge triggered J-K flip flops and explain its operation with timing diagrams.

Q6) Realize AND, OR, X-OR, X-NOR gates with the help of only NAND gates.

Section - C

(2 × 10 = 20)

Q7) Draw the circuit of a BJT RAM cell and explain its functioning with reference to read and write operation.

Q8) (a) Draw the circuit of a 4 bit counter type A/D convertor and explain its working.

(b) Obtain the minimal POS expression for the switching function given below using a four variable K-map.

$f(A, B, C, D) = T_1 (3, 4, 6, 7, 11, 12, 13, 14, 15)$.

Q9) Draw the circuit of 2 input TTL totem pole NAND gate and discuss its truth table. Discuss further :

(a) What are the advantages of using shottky TTL NAND gate?

(b) If the two inputs change their values at a very high frequency what impact it will have on the overall performance of the NAND gate.

(c) Merits and demerits of TTL over MOS gates.