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# B. Tech. (Sem. - 3rd)

## COMPUTER ARCHITECTURE

**SUBJECT CODE : CS - 201**

**Paper ID : [A0451]**

[Note : Please fill subject code and paper ID on OMR]

**Time : 03 Hours** **Maximum Marks : 60**

**Instruction to Candidates:**

1) Section - A is **Compulsory.**
2) Attempt any **Four** questions from Section - B.
3) Attempt any **Two** questions from Section - C.

## Section - A

**Q1)** *(10 × 2 = 20)*

a) How many 128 × 8 memory chips are needed to provide a memory capacity of 4096 × 16?

b) Simplify the following Boolean function using three variable K - Map.

$F(x, y, z) = \sum(1,2,3,6,7)$

c) An 8 - bit register contains the binary value 10011100. What is the register value after arithmetic shift right?

d) Represent the following conditional control statement by two register transfer statements with the control functions.

If (P = 1) then (R1 ← R2) else if (Q = 1) then (R1 ← R3)

e) What are the two instructions needed in the basic computer in order to set the E Flip flop to 1?

f) Write a symbolic Microprogram for the ADD operation.

g) Given the 16 bit value 1001101011001101. What operation must be performed in order to clear to 0 the first eight bits?

h) What are the different types of hazards in case of instruction pipeline?

i) List four peripheral devices that produce an acceptable output for a person to understand.

j) What is the transfer rate of an eight track magnetic tape whose speed is

## Section - B

*(4 × 5 = 20)*

*Q2)* Describe Booth's multiplication algorithm.

*Q3)* A two - word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W + 1) is designated by symbol Y. The operand used during the execution of instruction is stored at address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses. If the addressing mode of the instruction is.

(a) Direct.

(b) Indirect.

(c) Relative.

(d) Indexed.

*Q4)* Explain the difference between hardwired control and microprogrammed control. Is it possible to have a hardwired control associated with the control memory?

*Q5)* The time delay for the four segments in a pipeline are as follows: $t_1 = 50ns$, $t_2 = 30ns$, $t_3 = 95ns$, and $t_4 = 45ns$. The interface registers delay time $t_r = 5ns$.

(a) How long would it take to add 100 pairs of numbers in the pipeline?

(b) How can we reduce the total time to about one - half of the time calculated in part (a)?

*Q6)* Draw the diagram for a common bus system using tri - state buffers and a decoder instead of multiplexers.

## Section - C

*(2 × 10 = 20)*

*Q7)* How the architecture of parallel processors is different from pipeline processors? Give the application areas of the both.

*Q8)* Describe various modes of data transfer. Why does DMA have priority over the CPU when request a memory transfer?

*Q9)* Write the significance of Cache memory. Discuss the various types of mapping procedures while considering the organization of cache memory.