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 $(10 \times 2 = 20)$

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Roll No. Total No. of Questions : 09]

Paper ID [CS201]

(Please fill this Paper ID in OMR Sheet)

Time : 03 Hours

[Total No. of Pages : 03

B.Tech. (Sem - 3rd)

COMPUTER ARCHITECTURE (CS - 201)

Maximum Marks : 60

Instruction to Candidates:

- Section A is Compulsory. 1)
- Attempt any Four questions from Section B. 2)
- Attempt any Two questions from Section C. 3)

Section - A

(01) Choose the correct or best alternative in the following:

- Which logic is known as universal logic? a)
 - NAND logic (ii) PAL logic (i)
 - (iv) Decoder logic (iii) MUX logic
- The time for which the D-input of a D-FF must not change after the **b**) clock is applied is known as

Set-up time. (i) Hold time. (ii)

(iv) Delay-time. (iii) Transition time.

How many memory chips of (128×8) are needed to provide a memory c) capacity of 4096 × 16?

(ii) 16 (i) 64 (iii) 32

(iv) None of these

In addition of two signed numbers, represented in 2's complement form generates an overflow if

- (ii) $A \oplus B = 0$ $\mathbf{A} \cdot \mathbf{B} = 0$ (i)
- (iv) A + B = 1(iii) $\mathbf{A} \oplus \mathbf{B} = 1$

Where A is the carry in to the sign bit position and B is the carry out of the **Sign bit** position.

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d)

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- e) Addition of $(1111)_2$ to a 4 bit binary number 'A' results:-
 - (i) Incrementing A (ii) Addition of $(F)_{H}$
 - (iii) No change. (iv) Decrementing A

In a microprocessor system, suppose, TRAP, HOLD, RESET Pin got activated at the same time, while the processor was executing some instructions, then it will first respond to

- (i) TRAP (ii) HOLD
- (iii) RESET (iv) None
- g) Pseudo instructions are
 - (i) Machine instructions. (ii) Logical instructions.
 - (iii) Micro instructions. (iv) Instructions to assembler.
- h) An attempt to access a location not owned by a Program is called
 - (i) Bus conflict. (ii) Address fault.
 - (iii) Page fault. (iv) Operating system fault.
- i) Briefly write about 8255 chip.
- j) Compare SPMD and MIMD machine.

Section - B

$(4 \times 5 = 20)$

- **Q2)** A RAM chip 4096×8 bits has two enable lines. How many pins are needed for the integrated circuit Package? Draw a block diagram and label all input and outputs pins of the RAM. What is the main feature of random access memory?
- *Q3)* The RAM IC as described above is used in a microprocessor system, having 16 bit address line and 8-bit data line. It's enable- 1 input is active when A_{15} and A_{14} bits are 0 & 1 and enable-2 input is active when A_{13} , A_{12} bits are 'X' and 'O'. What shall be the range of addresses that is being used by the RAM.
- (1) Give the comparison between & examples of hardwired control unit and microprogrammed control unit.
- (3) What do you mean by Fetch cycle, instruction cycle, machine cycle, interrupt acknowledgement cycle.

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