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Printed Pages : 2

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BT–7/D12

VLSI DESIGN

Paper–ECE-401-E

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions by selecting at least **one** from each unit.*

Unit–I

1. (a) With proper illustrations show how a transistor is fabricated in a LOCOS, self-aligned E/D NMOS process. 12

(b) Write the equation of threshold voltage of a NMOS transistor and explain each term. 8

2. What is the need of stick diagrams ? Draw a stick diagram of a 1-bit full adder cell in a single poly, single metal N-Well CMOS process. Assume all inputs and outputs to be in poly running vertically from top to bottom on same x coordinate, Power lines to be horizontally running in metal. Give legend. 20

Unit–II

3. (a) What are the limits to scaling ? Discuss. 10

(b) Discuss the complete scaling theory. 10

4. (a) What do you understand by Layout methodologies ? Discuss. 10

(b) Discuss the various packaging techniques used by IC industry. Also discuss the merits and demerits of each. 10

Unit–III

5. (a) What is floor planning ? What are the objectives of floor planning ? 10

(b) Discuss one placement algorithm. 10

6. What is Kernighan-Lin algorithm ? How can one use the algorithm for a vertex set with an odd number of elements $2n + 1$ elements ? What about a situation in which the sets do not need to have the same size but may differ by at most m elements ? 20

Unit–IV

7. Discuss the Timing driven Placement and Routing. Discuss the critical issues involved and algorithms used to tackle them. 20

8. Discuss the following : 20

(a) Delay Models

(b) Timing driven routing via minimization.