Roll No. ..... Total Pages : 2

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BT-7/D09

VLSI DESIGN

Paper : ECE-401(E)

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *five* questions by selecting at least *one* question from each section.

SECTION–I

1. (a) Describe the NMOS IC fabrication with its process sequence and also discuss mask requirements. 10

(b) Describe the various electrical properties of CMOS inverter. 10

2. (a) Describe NMOS inverter transfer characteristics. 10

(b) Describe design rules in context to MOS design process with diagram and explain their significance. 10

SECTION–II

3. (a) What do you mean by delay in MOS circuits ? Explain how it effects the circuit operation with necessary expressions. 8

(b) What do you mean by the layout of a circuit ? Explain basic layout methodologies. 12

4. (a) Discuss the concept of circuit abstraction and its significance in layout design rules. 10

(b) Explain various Packaging techniques that are adopted in VLSI systems. What are the key factors that are to be taken care of during packaging a MOS device ? 10

SECTION–III

5. (a) Discuss Simulated annealing approach for placement. 10

(b) Discuss Rectangular dual graph approach to floor planning ? 10

6. (a) Describe basic fundamentals of Routing. Explain switchbox routing in detail. 10

(b) Describe routing in Row-based FPGAs. 10

SECTION–IV

7. (a) Describe Zero stack algorithm in timing driven placement issue in context of circuit layout performance. 10

(b) Describe delay in RC trees for CMOS VLSI circuit with example. 10

8. (a) Describe with example when to use Constrained *via* Minimization. 10

(b) Explain Buffered clock trees in timing driven routing. 10