Roll No. .....

8717

Printed Pages : 3

BT–7 / M 12

VLSI DESIGN

Paper–ECE–401–E

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt any **five** questions, selecting at least **one** from each unit.*

Unit–I

1. (a) Describe with illustrations, the two-metal n-well CMOS fabrication process to show how a CMOS inverter is fabricated. List all the masks in sequence of usage.

   (b) Discuss the voltage transfer characteristics of E/D NMOS inverter. 20

2. (a) Derive the drain current equation for a MOS transistor. What is channel length modulation ? 10

   (b) Draw the stick diagram of a 1-bit full adder in E/D NMOS technology. 10

Unit–II

3. (a) Why do we get progation delays ? For the CMOS fabrication process with device parameters as : $\mu_n.C_{OX} = 120\ \mu A/V^2$, $\mu_p.C_{OX} = 40\ \mu A/V^2$, $L = 0.6\ \mu m$, $V_{T0,n} = 0.8\ V$, $V_{T0,P} = -1.0\ V$, $V_{DD} = 3\ V$, $W_{min} = 1.2\ \mu m$. Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the propagation delay times $\tau_{PHL} \leq 0.2$ ns and $\tau_{PLH} \leq 0.15$ ns. Assuming the output load capacitance of 0.2 pF and ideal step input. 10

(b) What is packaging ? Discuss various packaging technologies. 10

4. Comparing the two scaling theories, constant-E and constant-V, show analytically by using equations how the delay time, power dissipation, power density, power-speed product are affected in terms of the scaling factor S. Which theory is more suitable for smaller geometries ? 20

Unit–III

5. What do you understand by routing ? Discuss the various routing algorithms. What is the grid model for global routing ? 20

6. Discuss the various Partitioning Algorithms. Discuss the advantages and disadvantages of each. 20

Unit–IV

7. Describe the delay models in Physical Design. How are timing constraints applied ? 20

8. Write short notes on :

   (a) Delay models in physical design. 10

   (b) Timing minimization. 10