8708

BT-7/M-15

VLSI DESIGN

ECE-401-E

Time : Three Hours] [Maximum Marks : 100

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) Describe the fabrication process steps for the fabrication of NMOS transistors and highlight the mask requirements.

(b) How the inversion voltage is affected by the relative sizes of the nMOS and pMOS transistors of the CMOS transistors of the CMOS inverter ?

2. (a) Find out the noise margin of a CMOS inverter.

(b) Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics.

Unit II

3. (a) Draw the circuit for 2-input NAND gate and its layout diagram giving explanations.

(b) Describe circuit abstractor.

4. Explain Colour coding concept used in stick diagram and describe Lambda based design rules and discuss their significance.

Unit III

5. (a) What is Routing problem in Physical VLSI circuit design ? Describe the various issues in Pin assignments.

(b) Explain the various approaches for Power and Ground Routing. Also describe planar routing and mesh routing issues in VLSI design.

6. (a) Describe framework used for multilevel partitioning problems. Explain with the help of suitable examples how clustering helps in the partitioning of multilevel problems ?

(b) What are the objectives of the Floorplanning and why optimization is essential in the design of physical VLSI circuit ?

Unit IV

7. What is Clock Skew Problem and how does it occur ? Explain the various methods that can be employed to prevent the problem of clock skew.

8. Describe the various power minimization techniques used in VLSI design.