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Total Pages: 2

BT-4/M-13

8401

COMPUTER ARCHITECTURE AND ORGANIZATION Paper : CSE-202(E)

Time: Three Hours]

[Maximum Marks: 100

Note: Attempt five questions in all, selecting at least one question from each unit.

UNIT-I

- 1. (a) What is Microprocessor? Compare and contrast the characteristics of RISC and CISC based processor.
 - (b) What is Instruction set? Discuss data transfer instructions of 8086.
- 2. (a) Explain Flynn's Classification of computers. 10
 - (b) What do you mean by Computer performance?

 Discuss any two metrics to measure performance of a computer system. Also, discuss pros and cons of these metrics.

UNIT-II

- 3. (a) Draw a diagram for a data path of a register based CPU, and explain the diagram.
 - (b) What is Instruction cycle? Give an example of 5-stage instruction cycle.
- 4. (a) What is the purpose of CU? Discuss micro-programmed CU.
 - (b) What is Microinstruction? Explain sequencing of microinstruction.

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|-------------------|---|-----------------------------|----------------|
| | UNIT-III | 137. 539. | An St |
| 5. (48) | What is Memory hierarchy? Discuss the | e characteristi | CS |
| 20 | of memory hierarchy. | e contract | 10 |
| (b) | Differentiate between SRAM and DRA | AM. | 10 |
| | Life mino verby sal | 1 9916 VA | |
| 6. (a) | How does cache improve performance | of a compu | ter |
| | system? Explain Direct-mapped cach | he organization | on. |
| | What are its limitations? | or trott | 10 |
| (b) | Distinguish between Paging and Segn | nentation. | 10 |
| | | | |
| | UNIT-IV | | 0 |
| 7. (a) | What is Instruction level parallelism | e ? Explain | he |
| | principle of instruction pipelining. | ACT | 10 |
| 75 3.471 | | ? Compare s | |
| (b) | What is Processor level parallelism | : Compare a | ına |
| (p) | | | |
| (b) | contrast a Multiprocessor and | Multicompu | |
| (b) | contrast a Multiprocessor and | | ter |
| 91164 | contrast a Multiprocessor and lassem. | Multicompu | ter 10 |
| 8. Ex | contrast a Multiprocessor and system. Applain the following with respect of 80×8 | Multicompu 36 processors | ter 10 |
| 8. Ex (a) | contrast a Multiprocessor and lasystem. Applain the following with respect of 80×8 Processor registers. | Multicompu 36 processors | ter 10 |
| 8. Ex | contrast a Multiprocessor and lasystem. Applain the following with respect of 80×8 Processor registers. | Multicompu 36 processors | ter 10 : |
| 8. Ex (a) | contrast a Multiprocessor and system. Aplain the following with respect of 80×8 Processor registers. Interrupts. | Multicompu 36 processors | ter 10 : |
| 8. Ex (a) (b) | contrast a Multiprocessor and system. Aplain the following with respect of 80×8 Processor registers. Interrupts. | Multicompu 36 processors | ter 10 : |
| 8. Ex (a) (b) | contrast a Multiprocessor and system. Aplain the following with respect of 80×8 Processor registers. Interrupts. | Multicompu 36 processors | ter 10 : |
| 8. Ex (a) (b) | contrast a Multiprocessor and system. Aplain the following with respect of 80×8 Processor registers. Interrupts. | Multicompu 36 processors | ter 10 : |
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| 8. Ex (a) (b) | contrast a Multiprocessor and system. Aplain the following with respect of 80×8 Processor registers. Interrupts. | Multicompu 86 processors | ter 10 : |
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