(Please write your Exam Roll No.) Exam Roll No. 60225602814

END TERM EXAMINATION

SIXTH SEMESTER [B.TECH] MAY-JUNE 2017

Paper Code: ETEC-308 **Subject: VLSI Design**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt all questions as directed. Internal choice is indicated.

Data: $k=1.38*10^{-23}J/K$, $q=1.6*10^{-19}C$, $n_i=1.45*10^{10}cm^{-3}$, $\varepsilon_0=8.85*10^{-14}$ F/cm, $\varepsilon_{si}=11.7\varepsilon_0$F/cm, $\varepsilon_{ox}=3.97\varepsilon_0$F/cm

Q1 (a) Derive an expression for depletion region depth at the onset of surface inversion in a MOS structure. **(5)**

(b) Discuss in brief the latchup in bulk CMOS and how to prevent it. **(5)**

(c) Discuss the charge-sharing problem in VLSI circuits, suggest one method to overcome charge sharing problem. **(5)**

(d) Consider a CMOS inverter with following parameters: **(5)**
nMOS $V_{TO,n}=0.6V$ $\mu_nC_{ox}=60\ \mu A/V^2$
pMOS $V_{TO,p}=-0.7v$ $\mu_PC_{ox}=25\ \mu A/V^2$
The power supply voltage is $V_{DD}=3.3V$. The channel length of both transistors in $L_n=Lp=0.8\mu m$. Determine the (W_n/W_p) ratio so that the switching threshold voltage of the circuit is $V_{th}=1.4V$.

(e) Explain the working of Zipper CMOS circuit. **(5)**

UNIT-I

Q2 (a) Briefly discuss basic steps of LOCOS process and what is the need for such process. **(5)**

(b) Explain the working of CMOS inerter clearly mentioning various regions of operation with neat graph and derive the expression for V_{IL} and V_{IH}. **(7.5)**

OR

Q3 (a) Consider a MOSFET with parameters: $t_{ox}=200A°$, $\Phi_{GC}=-0.8V$, $N_A=2*10^{15}$ cm^{-3}, $Q_{ox}=q.2*10^{11}$ C/cm^2, determine the threshold voltage V_{TO} under zero substrate bias at room temperature (T=300K) **(5)**

(b) Derive an expression for drain current in an NMOS transistor and discuss in detail the effect of channel length modulation on current-voltage characteristics. **(7.5)**

UNIT-II

Q4 (a) Derive an expression for propagation delay times by solving state equation of CMOS inverter with neat labeled waveforms. **(7.5)**

(b) Implement XNOR gate and 2:1 MUX using transmission gate. **(5)**

OR

Q5 (a) Explain the biasing conditions and operating regions of transmission gate, also obtain the expression for equivalent resistance in different regions of operation. **(6)**

(b) Explain the working of CMOS NOR2 gate and derive the expression for switching threshold voltage V_{th}. **(6.5)**

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UNIT-III

Q6 (a) Draw the CMOS circuit of AOI-based implementation of "clocked NOR-based SR latch" circuit and describe the working with required waveforms. **(6)**

(b) Explain how voltage bootstrapping helps enhancement-type circuit in which the output node is weakly driven. **(6.5)**

OR

Q7 (a) Draw the "CMOS AOI realization of JK latch" and explain its working. **(6)**

(b) Differentiate between ratioed logic and ratioless logic using "dynamic shift register". **(6.5)**

UNIT-IV

Q8 Write a short note on the following-

(a) VLSI Design flow **(4.5)**

(b) Full Custom Design **(3)**

(c) Concept of regularity, modularity and locality with example **(5)**

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