(Please write your Exam Roll No.) Exam Roll No. 6022560 2814

END TERM EXAMINATION

THIRD SEMESTER [B.TECH.] DECEMBER 2015

Paper Code: ETEC-205 **Subject: Switching Theory & Logic Design**

Time: 3 Hours **Maximum Marks: 75**

Note: Attempt any five questions including Q no.1 which is compulsory. Internal choice is indicated.

Q1 (a) Convert the Hexadecimal number 68BE to Binary and then convert it to Octal. **(2)**

(b) Explain Cary look Ahead Adder with Diagram. **(3)**

(c) Subtract the following binary No's: **(2)**

(i) 10110-1011

(ii) 1100.10-111.01

(d) Why Exces-3 known as self-complementing code? Explain with example. **(2)**

(e) What is the drawback of JK flip-flop? **(2)**

(f) What are the advantages of CMOS? **(3)**

(g) Implement function $F(a,b,c) = ab + \bar{b}c$ using 4:1 Mux. **(3)**

(h) Difference between Mealy and Moore models. **(2)**

(i) How ASM chart is different from Flowchart? **(2)**

(j) Explain in brief about Fault models of Sequential circuits. **(2)**

(k) What do you mean by the term State Table? Explain with Example. **(2)**

Q2 (a) Obtain the minimal expression using Tabular method and implement it in universal logic **(7.5)**

$F = \sum m(1,5,6,12,13,14) + d(2,4)$

(b) Explain with the help of circuit diagram binary to Excess-3 code converter. **(5)**

OR

Q3 (a) Discuss the difference between PLA and PAL. **(2.5)**

(b) With the help of equations explain 4 bit comparator. **(5)**

(c) Implement the following multiple output combinational logic circuit using a 3-to-8 line Decoder? **(5)**

(i) $F1 = \sum m(0,1,2,6)$

(ii) $F2 = \sum m(2,4,6)$

(iii) $F3 = \sum m(0,1,5,6)$

Q4 (a) Show the characteristic equation for the complement output of a JK flip-flop is **(4)**

$\bar{Q}(t+1) = \bar{J}\bar{Q} + KQ$

(b) Explain four bit Bi-directional Register with the help of Multiplexers. **(5)**

(c) Explain the characteristic of TTL logic family. **(3.5)**

OR

Q5 (a) Design a decade synchronous UP counter. Use T flip-flops **(7)**

(b) With the help of circuit diagram, explain CMOS logic gate. **(2.5)**

(c) Explain Twisted Ring counter with the help of Timing Diagram. **(3)**

Q6 (a) Design a sequence detector that will detect the sequence 1011 and sequence should be Overlapping. **(7.5)**

(b) Explain capabilities and Limitations of FSM. **(5)**

OR

Q7 (a) For the state table given below, find the equivalence partition and corresponding reduced machine in standard form. **(4.5)**

Present State	Next State, Z	
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

(b) For the state table given below, find the set of maximal compatibles using- **(8)**
(i) Merger graph method
(ii) Merger table method

PS	Next State			
	I0	I1	I2	I3
A	C,0	-	C,0	-
B	A,-	B,1	C,-	-
C	-	C,0	-,1	D,0
D	F,0	-	E,1	C,-
E	F,0	-	A,-	C,1
F	-	B,1	-,0	B,1

Q8 (a) Draw the ASM chart for the following state transitions. Start from initial state T1, then, if xy=00 go to T2, if xy=01 goto T3, if xy=10 goto T1, otherwise goto T3 and Design its control unit using Multiplexers.**(7.5)**
(b) Explain different fault detection experiments in sequential circuits. **(5)**

OR

Q9 (a) Draw the state Diagram, state Table and the ASM chart for a 3 bit down counter. The circuit should generate an output 1 whenever the count becomes minimum or maximum. **(6.5)**
(a) Write short notes on the following:- **(2x3=6)**
(i) Homing Experiments
(ii) Distinguishing Experiments.

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P2/2