1153070

24043

B.Tech. 3rd Semester (I.T.) Examination,
December–2016

DIGITAL ELECTRONICS

Paper–EE–204–F

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *The candidate will be required to attempt* ***five*** *questions in all at least* ***one*** *question from each unit.*

Question No. 1 is compulsory.

1. (a) What is meant by parity bit ? 1

(b) Define duality property. 1

(c) State De Morgan's theorem. 2

(d) What is encoders and decoders ? 4

(e) Define sequential circuits and latches. 2

(f) Difference between latches and flip flop. 2

(g) What is the difference between PLA and PAL ? 2

(h) What is the asynchronous sequential logic ? 2

(i) Explain hamming codes with example. 2

(j) Define binary codes, cyclic codes, error detecting and error correcting codes. 2

Unit–I

2. (a) Design a simple logic circuit such that the output is 1 when the binary numbers A, B, C, D is greater than 0110. 8

(b) In a 4-input NAND gate, two inputs are to be used. What are the options available for the unused inputs and which one is the best and why ? 7

(c) What is prime implicants ? and state distributive law. 5

3. (a) Perform the following operations on the given binary numbers a specified :

(i) 110.01 + 1.011 1

(ii) Convert 11101.01 to decimal 1

(iii) 11100.101–101.01 using 2's compliment. 1

(iv) State whether the following statement is true or false :

"All decimal fractions have exact binary equivalents" and justify your answer. 2

(b) Solve the following expression by mapping :

$F = \Sigma m (0, 2, 3, 6, 7, 8, 9, 10, 13)$.

Write the steps involved in solving this Quine-McClusky method. 7

(c) Perform the operation $(12_{10} - 35_{10})$ using 2's compliment method. 2

(d) Obtain the minimal SOP expression for

$Y (A, B, C, D) = \in m (2, 3, 5, 7, 8, 9, 11, 12, 13, 14, 15) + d (2, 4)$ using k-map. Realize the expression using 2-input NAND gates only. 6

Unit–II

4. (a) Construct a 4-input multiplexer using four 3-input AND gates, an OR gate and three inverters. Show the input, output and select lines and write a table showing the outputs for various select inputs. 8

(b) Design a combinational circuit that accepts a 3-bit number as input and generates an output binary number equal to square of the input number. 5

(c) Implement a four variable function :

$F(A, B, C, D) = \in (0, 1, 3, 4, 8, 9, 15)$.

Using an 8×1 multiplexer. 7

5. (a) How will you obtain 8 to 1 mux from 4 to 1 mux's ? 4

(b) Explain 4-bit magnitude comparator with diagram. 8

(c) Design a combinational circuit with three inputs and one output. The output is equal to logic-1 when the binary value of the input is less than 3. The output is logic-0 otherwise. 8

Unit–III

6. (a) What two types of input does a clocked FF have ? Explain. What is meant by edge triggering ? Define set-up time and hold-time for a clocked FF. 8

(b) Design a mod-7 asynchronous up-counter using JK flipflops. Write the state diagram

and the timing diagram for the same. The counter counts during +ve edges of the clock. 7

(c) Write the counting sequence of a 4-bit down synchronous counter. Design the same by using –ve edge triggered J-K flip-flops. 5

7. (a) What is the twisted ring counter ? Write a 4-bit twisted ring counter. Explain its operation giving the states. 8

(b) Implement a 4-bit serial-in serial-out shift register using D flipflops and raw the output waveform for an input 1010. 4

(c) A binary ripple counter is required to count up to $(16383)_{10}$. How many flip flops are required ? If the clock frequency is 10.5 mhz, what is the frequency at the output of msb ? 4

(d) What is race around condition in a J-K flip flop ? Explain how it occurs ? Suggest a method to overcome the race around difficulty. 4

Unit–IV

8. (a) Obtain the ASM charts for the following state transitions :

(i) If x = 0, control goes from state T_1 to state T_2 : if x = 1, generate a conditional operation and go from T_1 to T_2.

(ii) If x = 1, control goes from T1 to T2 and then to T3 : If x = 0, control goes from T1 to T3.

(iii) Start from stte; then : if xy = 00, go to T2; if xy = 01 go to T3; if xy = 10 go to T1; otherwise, go to T3. 12

(b) What is race free state assignment ? 3

(c) Explain how the ASM chart differs from a conventional flow chart. 5

9. (a) Design a digital system with three 4-bit registers, A, B and C, to perform the following operations :

(i) Transfer two binary numbers to A and B when a start signal is enabled.

(ii) If A < B, shift left the contents of A and transfer the result to register C.

(iii) If A > B, shift right the contents of B and transfer the result to register C.

(iv) If A = B, transfer the number to register C unchanged. 12

(b) Prove that the multiplication of two n-bit numbers gives a product of length less than or equal to 2n bits. 8