**

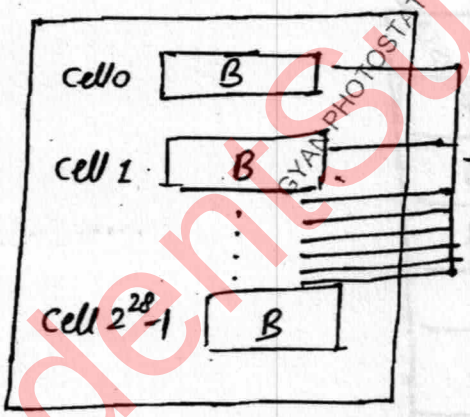
Que Consider a 64 bit hypothetical Processor which supports 256 MB m/y processor is enhanced with a word addressible m/y unit. How many Number of address pins are saved in the New CPU to address the m/y unit.

$256\ MB = 2^8 \times 2^{20} \times \frac{8}{64} = 2^{25}$ cells

$2^{28}/2^{25} = 2^3 \Rightarrow$ 3 pins

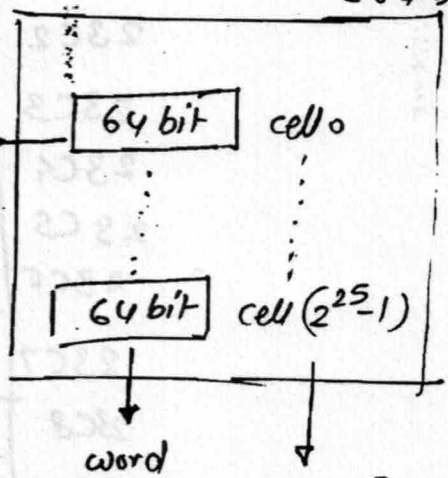
System old

256 MB m/y



Word Addressible m/y

cell size = word size = 64 bit



bits save = (28 - 25)

= (3)

Que:- A hypothetical m/y chip IC contain 28 Address Pins and 64 data Pins what is the capacity of m/y in Bytes.

$2^{28} \times 2^{64}$ bits $\Rightarrow$ ~~256 GB~~ $2^{28} \times 8B \Rightarrow 2^{31}B$

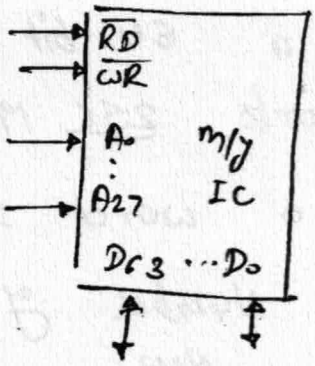
m/y size = 2^{28} cells

$= 2^{28} \times 64$ bits

$= 2^{28} \times 8$ Bytes

$= 2^{31}$ Bytes

$= 2$ GB



Eg: Consider a 32 bit hypothetical Processor interfaced with a Byte Addressible m/y unit. CPU accessing the Data word from the m/y with a starting address of $(23C4)_H$ onwards m/y contents is as follows:

23C2	88
23C3	99
23C4	AA
23C5	BB
23C6	CC
23C7	DD
23C8	EE
23C9	FF

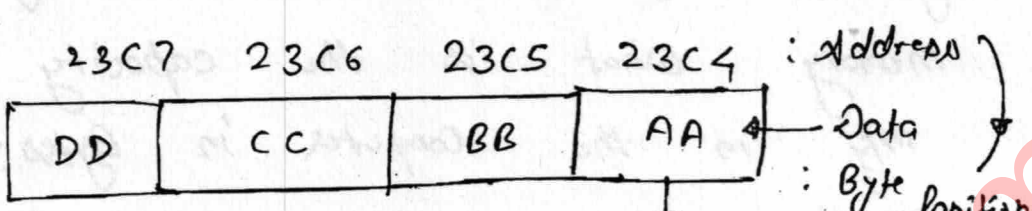
a) How many m/y cells will be interfaced

b) what is the Data word when the computer is designed with little-endion

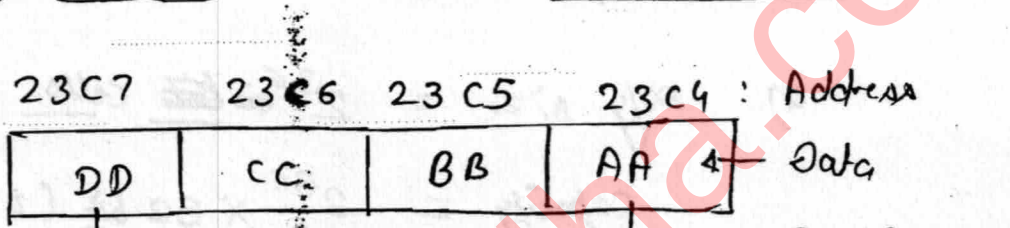
c) what is the data word when the computer is designed with Big-Endion.

a) 4 cells of 32 bit Processor

b) Little-Endian :



c) Big-Endian : Ans : DDCC BBAA



Ans : AA BB CC DD

Que:- A 64 bit Hypothetical Processor is interfaced with a Byte Addressible memory. Data word is present in the memory with a starting address of $(C4CDCFA4)_H$ what is the capacity of main memory in the computer. and How many cells are interfaced to a CPU.

a) $(C4CDCFA4)_H$

Address size = 32 bit

memory size = 2^{32} cells

= 2^{32} B ← m/y Byte Addressible

= 4GB

b) 8 cells

Que:- A 32 bit Hypothetical Processor is interfaced to a word addressible memory. CPU generates 36 bit Address to refer the memory what is the capacity of the m/y in the Computer in Bytes: and How many m/y cells are interfaced to a n CPU.

a) m/y size = 2^{36} cells

capacity = 2^{36} X 32 bit (1 word)

= 2^{36} * 4B (cell size)

= 2^{38} = 256 GB

b) 1 cells interfaced (word Addressible m/y)

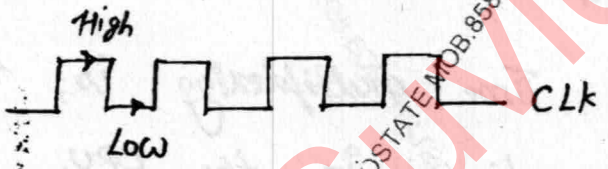
m/y capacity = # of cells * cell size

"CPU Pin Structure" :-

* Processor contain set of Hardware pins used to perform the operations on a externally connected components { memory and I/O }.

* Hardware Pins are categorized into three groups :

i) Active Low Pin,
ii) Active High Pin,
iii) Time multiplexed Pin



i) Active Low Pin :-

This Pin is enabled when the clock Pulse in the low state denoted as: $\overline{\text{Pin name}}$

eg: $\overline{RD}$
$\overline{WR}$
$\overline{INTA}$ etc.

ii) Active High Pin :-

This Pin is enabled when the clock pulse is in High state. denoted as: Pin name.

eg: ALE
INTR
HOLD
HLDA etc.

(iii) Time multiplexed Pin :-

This Pin is used to carry the address and data but not at the same time.

eg: In 8085;

AD_7 — AD_0

Address — Data.

eg: In 8086;

AD_{15} — AD_0

Address — Data

* Advantage of Time multiplexing is, reduces the Hardware pins in the CPU.

* 'ALE' Pin is used to differentiate the address and data. i.e.

ALE (Address Latch enable) Pin

0: Time multiplexed Pins carries the 'Data'

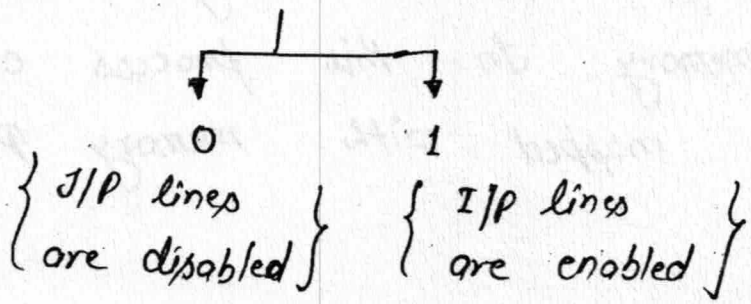
1: Time multiple Pins Carry the 'Address'

* "Address Latch" is used to lock the address.

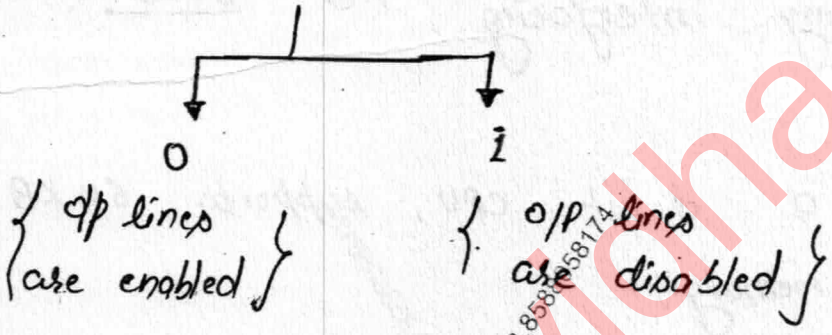
-: It contain two control Pins : two operate the latch :

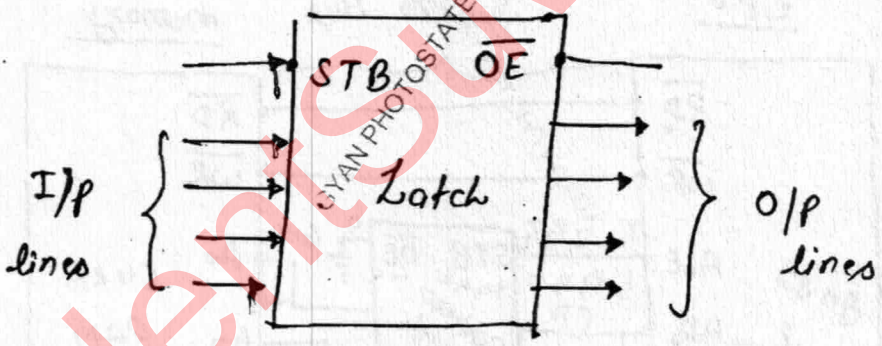
two controls Pins :-

① STB (Strobe) Pin



② $\overline{OE}$ ($\overline{O/P}$ enable) Pin





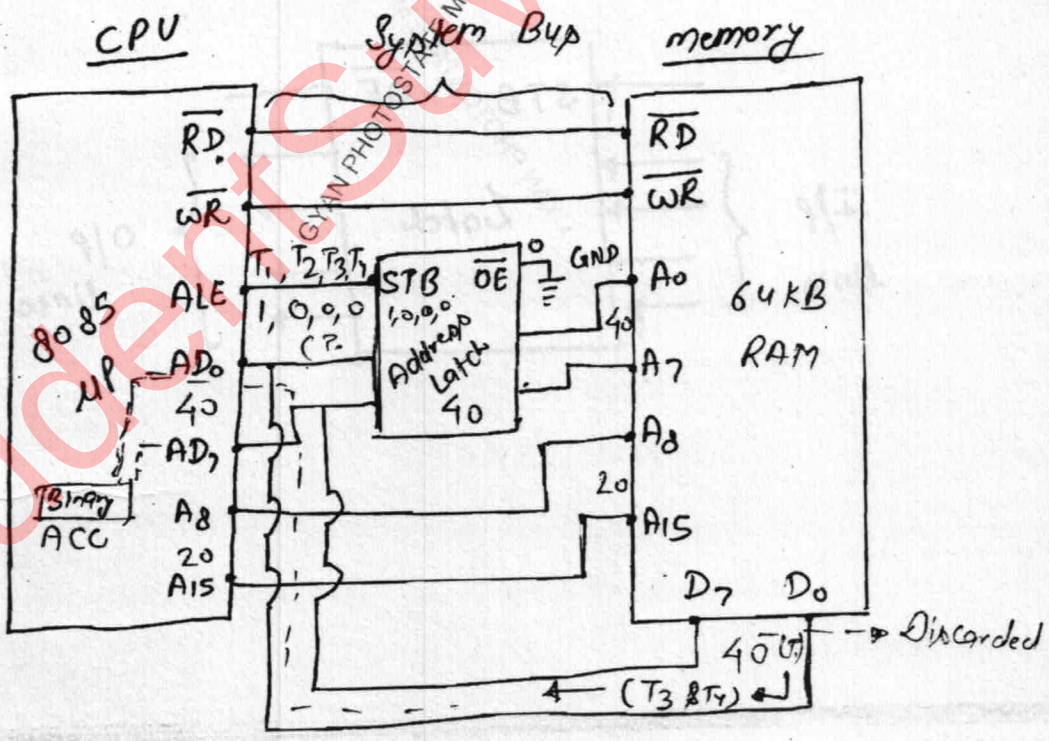
"Memory Interfacing" :-

This concept is used to integrate the cpu and memory. In this process cpu Pins are mapped with memory Pins respectively.

Let us consider a reference cpu to analyze the memory interfacing i.e 8085 (40 Pin cpu)

-: 8085;

It is a 8 bit cpu, supports 64 kB Physical memory.



:- 8085 µP

Machine Instⁿ : LDA [2040] → Load to Acc from m/y

↓

Acc ← m [2040]

↓

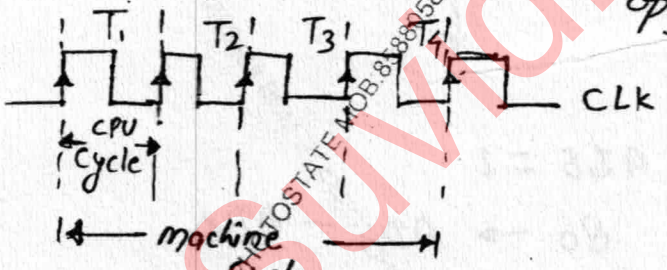
CPU generates the memory request

2040H	$\overline{RD}$

↓

machine cycle

{ # of CPU cycles required to complete the main memory operation }



Actions :-

① Send the "Address"

T_1 : ALE = 1

40 → $AD_7 - AD_0$

20 → $A_{15} - A_8$

② Send the 'CS' (control signal)

T_2 : ALE = 0

$\overline{RD}$ = 0

$\overline{WR}$ = 1

③ Read the "Data"

T_3 & T_4 : ALE = 0 $D_7 - D_0$ → $AD_7 - AD_0$

{ m/y Latency / m/y delay / m/y Access time }

i) machine : STA [4080] → Store into the m/y via Acc

Instⁿ

↓

m [4080] ← Acc

↓

CPU generates the memory Request

4080H	$\overline{WR}$

↓

machine cycle

{ T_1, T_2, T_3, T_4 }

↓

Actions :

T_1 : ALE = 1

80 → AD_7 — AD_0

40 → A_{15} — A_8

T_2 : ALE = 0

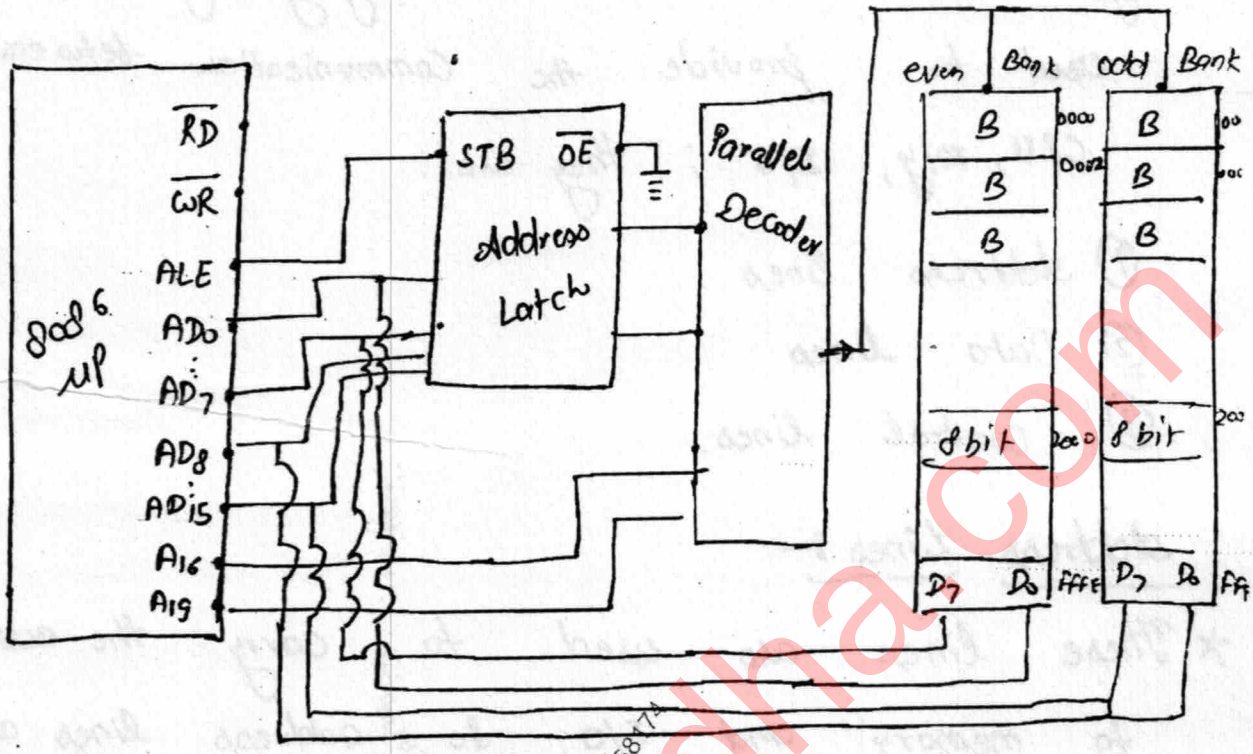
$\overline{RD}$ = 1

$\overline{WR}$ = 0

T_3 & T_4 : ALE = 0

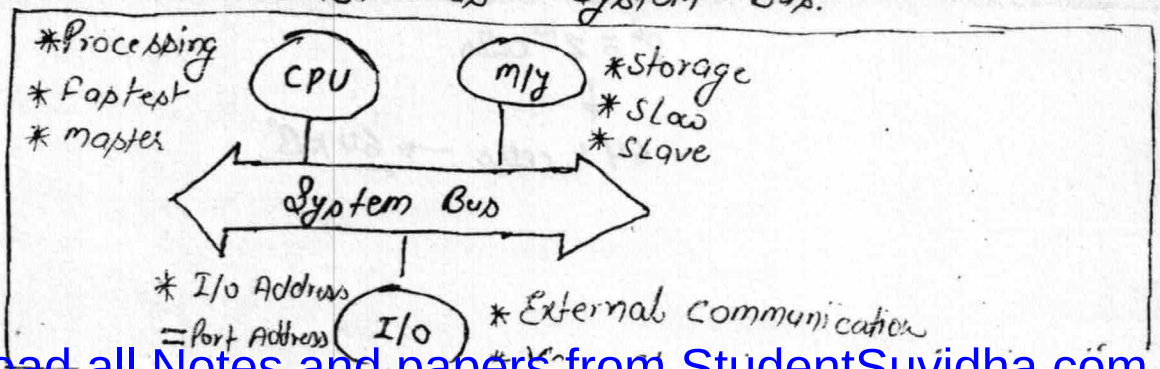
$AD_7 - AD_0 \rightarrow D_7 - D_0$

:- 8086 µP



System Bus Design :

* Bus is a communication channel
* Characterstic of a bus is : Shared transmission medium.
* Limitation of a bus is : only one transmission at a time.
* A Bus which is used to provide the communication between the major components of a computer is called as System Bus.



"computer" ⇒

* System Bus contain three category of lines used to provide the communication between CPU, m/y, I/O ; they are :

① Address lines
② Data lines
③ control lines.

Address Lines :-

* These lines are used to carry the address to memory and I/O. So address lines are uni-directional.

* Based on the Address lines, we can determine the capacity of a memory system.

eg :- In 8085 µP,

$A_{15} - A_8$, $AD_7 - AD_0$

↓

16 Address lines

↓

2^{16} cells

↓

$2^6 \times 2^{10}$ cells

↓

64 k cells → 64 kB

Eg 2: In 8086 µP,

$A_{19} - A_{16}$, $AD_{15} - AD_0$

↓

20 Address lines

↓

2^{20} cells

↓

1M cells → '1MB'

eg: In X-CPU, 38 Address lines are Present

then, MM size = 2^{38} cells

= 256 G cells → 256GB

* size of memory depends upon the address lines of the µ-Processor

Data Lines :-

* These lines are used to carry the binary sequence between the CPU, m/y and I/O so data lines are bi-directional.
* Based on the data lines, we can determine the word length of CPU.
* Based on the word length, we can measure the Performance of a CPU.

Data Lines :-

* Bi-directional
* word - Length
* Performance

eg: In 8085 up

$AD_7 - AD_0$

↓

8 Data Lines

↓

word length = 8 bit

↓

operations are performed on 8 bit data code.

eg: In 8086 up

$AD_{15} - AD_0$

↓

16 Data lines

↓

word length = 16 bit

↓

operation are performed on a 16 bit data code.

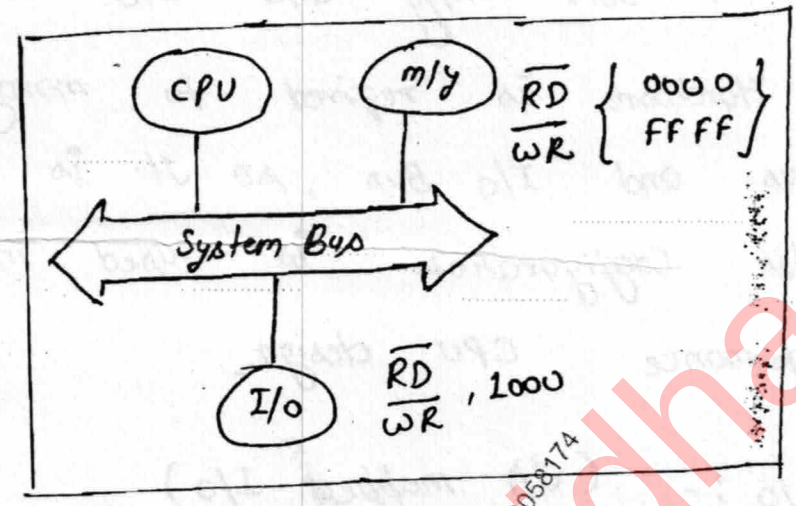
"control Lines" :-

* These lines are used to carry the control signals and timing (clock) signals.
* Control signals indicate the type of operation, and timing signals are used to synchronize the m/y and I/o operations with CPU clock.

Note :- when there is a common bus, Common control signal and common address space is used between the m/y and I/o then there is a

possibility of Ambiguity (Communication Problem)

* Common Bus
* Common CS
* Common Address



CPU generates the memory request

1000	RD

1000 → AL's
RD → CL's

m/y Controller: 1000 → valid, RD → valid } m/y op^n

I/O Controller: 1000 → valid, RD → valid } I/O op^n

Ambiguity

:- To Handle the above problem bus configurations are used in the system design.

Three different Bus configurations are used in computer design:

1. IOP [input-output Processor]
2. Isolated I.O [I/O mapped IO]
3. memory mapped IO.

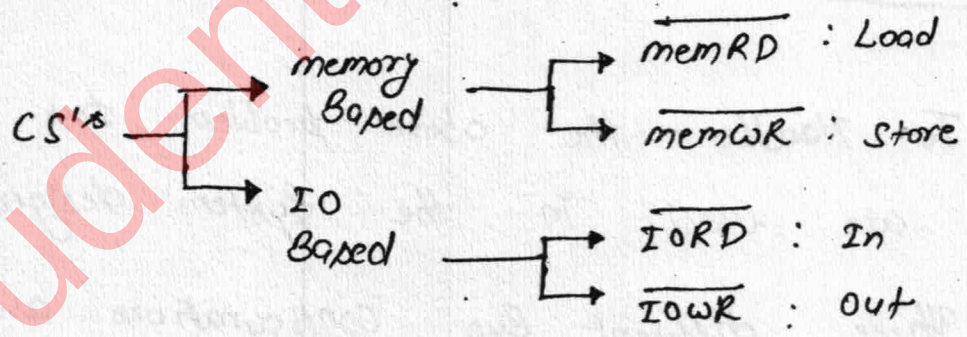
IOP :- (Input/output Processor)

★ This configuration uses common control signals and common address space but 'different buses' for both m/y and I/O.

★ Additional Hardware is required to manage the memory Bus and I/O Bus, so it is expensive therefore this configuration is used in the High performance CPU design.

Isolated I/O :- (IO mapped I/O)

★ This configuration uses the common Bus and common address space but 'different control signals' for both memory and I/O.



★ IO/M Hardware Pin is used to implement isolated IO.

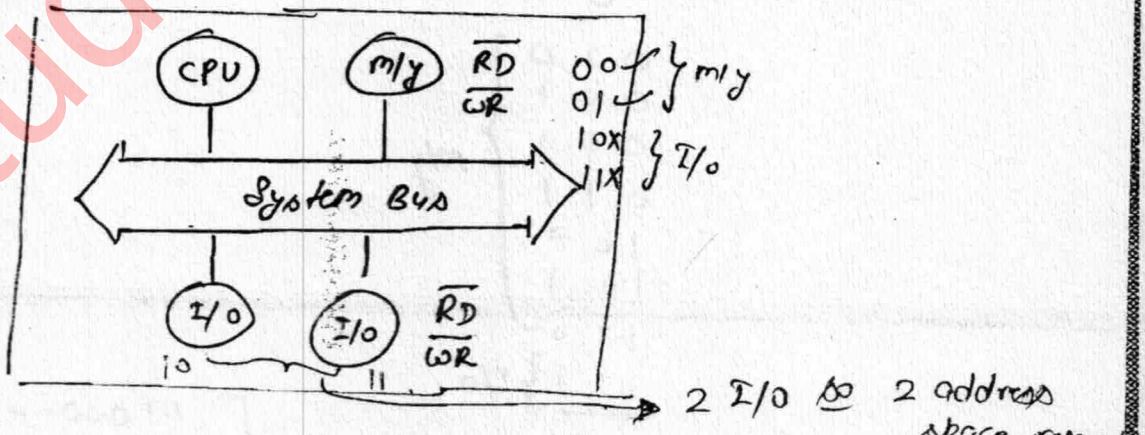
IO/M	RD	WR	CS
0	0	1	MemRD
0	1	0	MemWR
1	0	1	IORD
1	1	0	IOWR

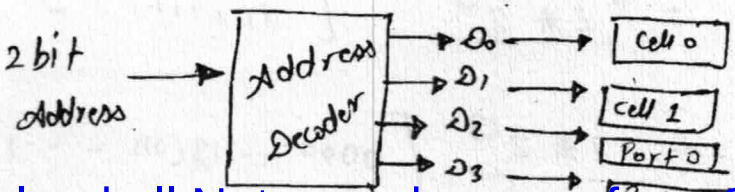
It is less expensive, used in the general purpose computer design.

memory mapped IO :-

★ This configuration uses the common bus, common control signals but 'unique address space for both memory and I/O.'

★ In this configuration, memory Address space is shared to IO. So limitation is complete memory space is not in the use.





Que:- Consider a hypothetical Processor which supports 64 kB memory. Processor uses the memory mapped I/O. in which when the 3 MSB bits of address is 1 then use them for I/O ports. How many number of Port addresses and m/y addresses are possible in the System.

Soln:- $64kB = 2^{16} = 16$ A.L. $f000$

3 MSB bits.

memory size = $\frac{64kB}{64k \times 8}$

$\log_2 2^{64} = 16$ bit

Address :- $A_{15}\ A_{14}\ A_{13}$ (3 bit) $A_{12}\ A_{11}\ \cdots\ A_0$ (13 bits)

000
001
010
011
100
101
110 } m/y
111 } I/O

Port Address = $1 * 2^{13}$ [111 000 -- (13)0's
111 111 -- (13) 1's]

memory Address = $7 * 2^{13}$ [0000 -- 13 0's -- 110 ---

Que:- Consider a Hypothetical CPU which supports 2^{28} Byte memory space. System designed with a memory mapped I/O. in this configuration both of the addresses are seperated with a 6 MSB bits. In the 6 MSB bits combination, 8 combinations are used for I/O How many No. of I/O Ports are Possible in the system.

2^{28} Byte ⇒ 28 bit ⇒ Address lines

A_{27} A_{26} A_{25} A_{24} A_{23} A_{22} | A_{21} A_{20} ... A_0

6 bit | 22

6 / I/O | 22

2^6 = 64 combination → 8 → I/O, 56 → m/y

I/O :- $8 * 2^{22}$ for I/O

Addresses ⇒ 2^{25}

* Que:- Consider the Hypothetical CPU which ~~supp~~ contain 34 Address Pins. Processor is Interfaced with a 8 cells of the m/y space. What is the capacity of the m/y System and word length of CPU.

capacity = 2^{34} cells * ~~64 bit~~ = 16 GB (default m/y is Byte Addressable)

= $2^{34} * 8$ = [illegible]

word length = 64 bit