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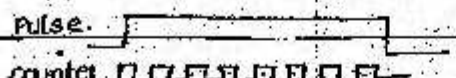
## ☆ COUNTERS :-

⇒ Counters are basically used to count no of clock pulse applied. it can also be used for frequency divider, & time measurement, frequency measurement, Range measurement, pulse width.




⇒ Also used for waveform generator.

⇒ With n-ff, max. possible stage in the counter is $2^n$

$$N \leq 2^n$$

or, $n \geq \log_2 N$

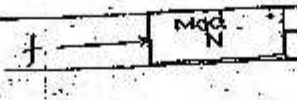
where N = no. of stage
n = no. of FF.

Depending on clock pulse applied counters of two type:

(i) Asynchronous
(ii) Synchronous.

| Asynchronous | Synchronous |
|---|---|
| 1. Different FF are applied with different clock. | 1. All FF are applied same clock, |
| 2. It is slower. | 2. It is faster |
| 3. Fixed count sequece ie. up or down. | 3. Any count sequence is possible |
| 4. Decoding errors will present | 4. No decoding error will present |
| 5. Ripple counter | 5. Ring counter |

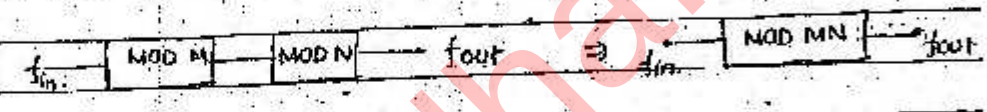
⇒ No. of stage use in counter mean modulus of counter.
i.e. if MOD 5 counter = 5 stage.
MOD n counter = n stage




Q: A decadde counter is applied with frequency of 10MHz then o/p frequency is...

Sol: $f_{out} = \frac{f_{in}}{10} = \frac{10\,MHz}{10} = 1MHz$

⇒ Let MOD M and MOD N are cascaded then it will act as MOD MN counter.




Content :-
- Basic
- Ripple counter
- Non binary ripple counter
- Ring counter
- Johnson counter
- Synchronous series carry
- Synchronous parallel carry
- Synchronous counter design and Analysis.

(A) Ripple counter :-
- ⇒ It is a Asynchronous counter.
- ⇒ Different FF used different clock pulse.
- ⇒ Toggle mode.
- ⇒ Only one FF is applied with external clk and other ff's are clk is from previous ff o/p. (whether Q or $\bar{Q}$)
- ⇒ The FF applied with external clk will acts as LSB bit.

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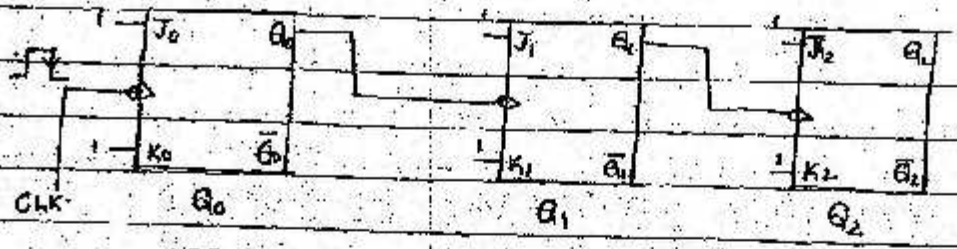
## 3 bit ripple counter :- (up counter)




(i) Explanation :-

⇒ The ckt shown in fig $Q_0$ toggle for every clk pulse

⇒ $Q_n$ change when $Q_{n-1}$ change from 1 - 0. i.e. $Q_1$ changes when $Q_1$ changes from 1 - 0.

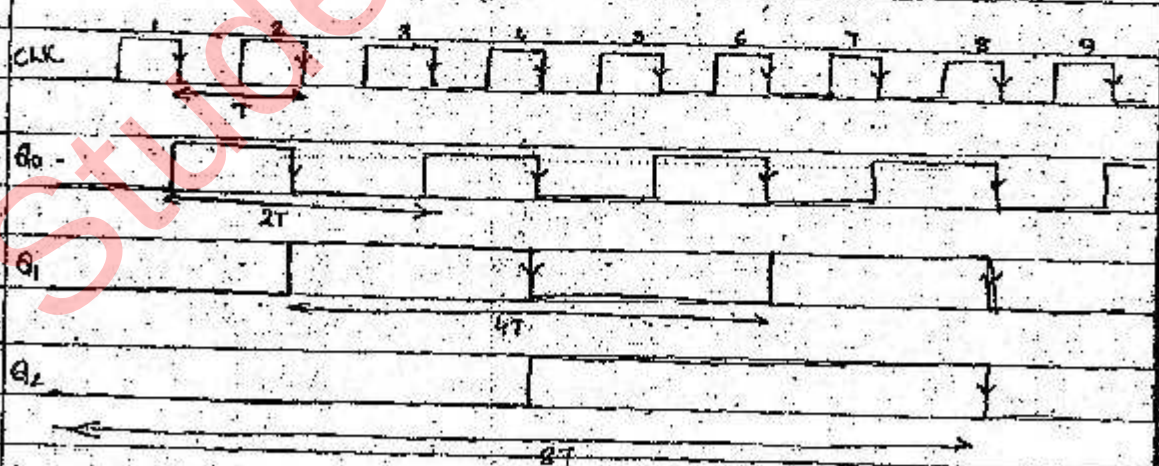
(ii) ⇒ Truth table :-

| CLK | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |

⇒ This is up counter.

⇒ It is also called MOD 8 ripple counter.

(iii) Timing Diagram :-

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⇒ In n bit ripple counter propogation delay of each ff is $t_{pdff}$. then time period of CLK is,

$$T_{clk} \geq n\, t_{pdff}$$

$$f_{clk} \leq \frac{1}{n\, t_{pdff}}$$

$$f_{max} = \frac{1}{n\, t_{pdff}}$$

Note:-

(i) -ive edge trigger → Q as clock → up counter
(ii) +ive " " → $\bar{Q}$ as clock → up counter.
(iii) -ive " " → $\bar{Q}$ as clock → down counter.
(iv) +ive " " → Q as clock → down counter.

3-Bit Ripple counter (Down counter):-


(i) Explanation :-

⇒ The ckt shown in fig. $Q_0$ toggles for every clock pulse.
⇒ $Q_1$ toggles when $Q_0$ changes from 0 to 1.
⇒ $Q_2$ toggles when $Q_1$ changes from 0 to 1.

(ii) Truth table:-

| Clock | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |
| 2 | 1 | 1 | 0 |
| 3 | 1 | 0 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 0 | 1 | 1 |
| 6 | 0 | 1 | 0 |
| 7 | 0 | 0 | 0 |

⇒ This is called ripple counter because the input clock is the o/p of previous FF output. this is just like ripple. then called Ripple counter.

⇒ if the o/p is (000) and clock is applied then $t_{pdf}$ is delay

000

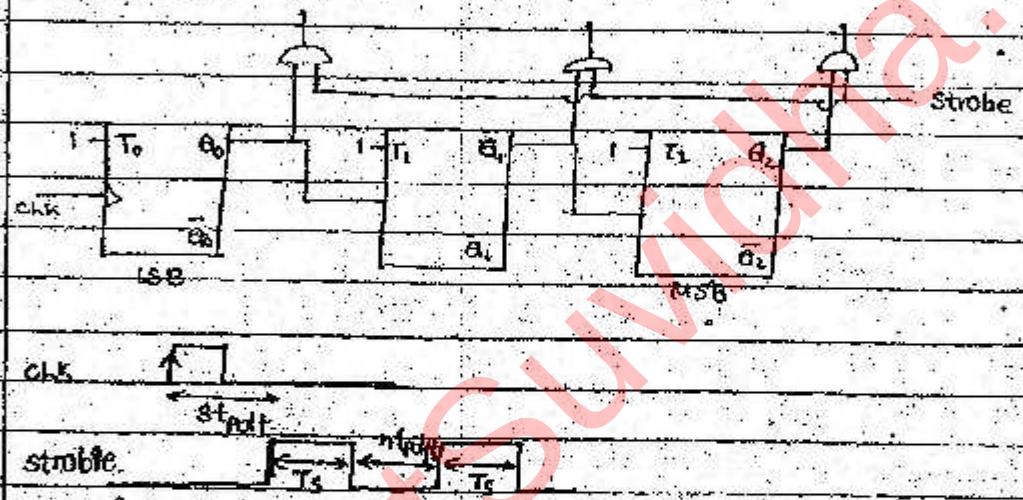
$t_{pdf}$ → 001 } unwanted or decoding error.

$t_{pdf}$ → 011 } also called transient state.

111

⇒ Decoding errors or transient state present in ripple counter due to propagation delay.

⇒ To avoid decoding error strobe signal is used.







⇒ i.e. strobe signal is zero for $nt_{pdff}$ and after that it is one for next clock. then all the o/p is zero for the transient time therefore due to strobe signal we can remove decoding error.

$$T_{CLK} \geq nt_{pdf} + T_s$$

⇒ In ripple counter with n ff max possible state is $2^n$.

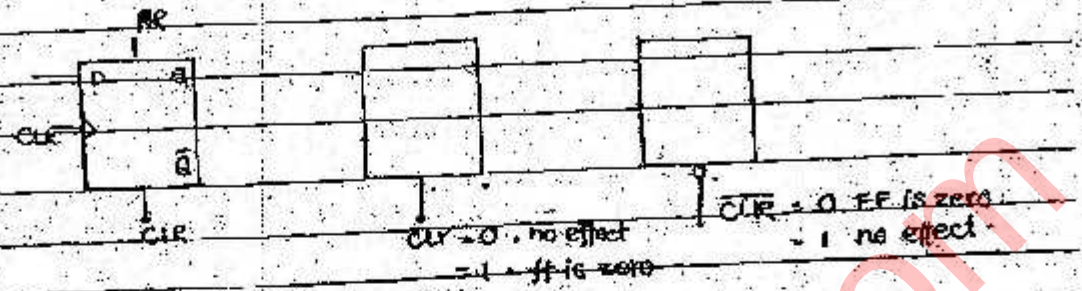
⇒ frequency after n FF in the Ripple counter is $f/2^n$. (ie. for 3 FF o/p is f/8)

⇒ Clear and preset are known as Asynchronous I/P.

S, R, J, K, D, T are Synchronous I/P.

Clear :- clear is use to rest our ff or counter.

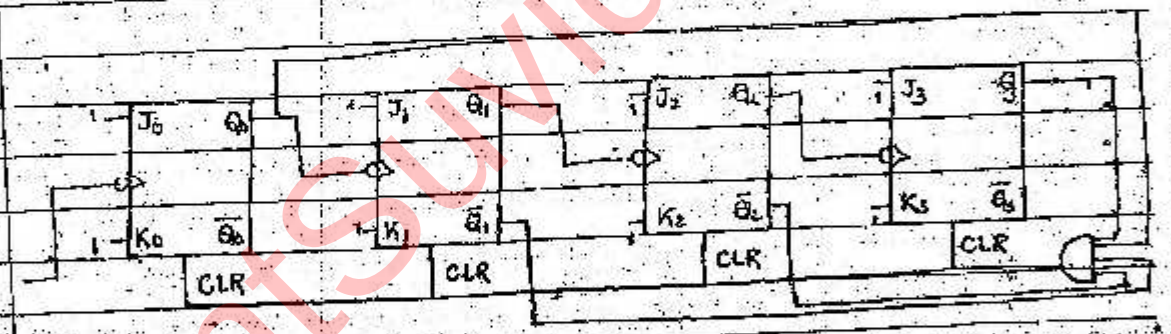
Preset :- preset is use to set our FF or counter.




(B) Non Binary Ripple counter :-

(B1) BCD counter :- (Decade counter)

⇒ 4 flip flop used.




| CLK | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

(1010)

$Q_3\bar{Q}_2Q_1\bar{Q}_0$

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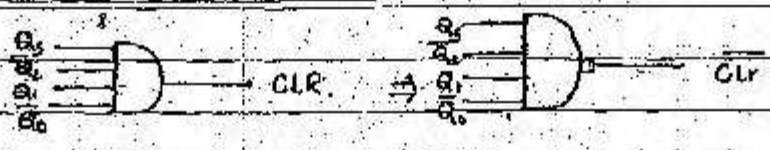
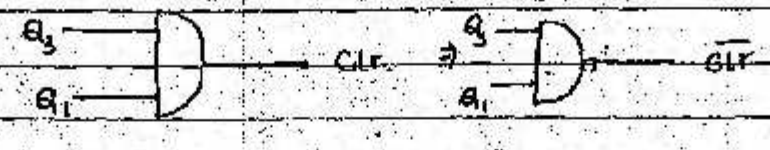



if we use only $Q_3$ and $Q_1$, we also use this as clear ckt.




$\Rightarrow$ All BCD counter is Decade counter but reverse is not true.

$\Rightarrow$ BCD counter is Asymmetric o/p time Diagram.

$\Rightarrow$ o/p frequency of BCD counter is $f/10$.

$\Rightarrow$ low for 8 clock and high for 2 clock in $Q_3$

$\Rightarrow$ duty cycle is 20%

Imp $\Rightarrow$ In Asynchronous counter follow steps:-

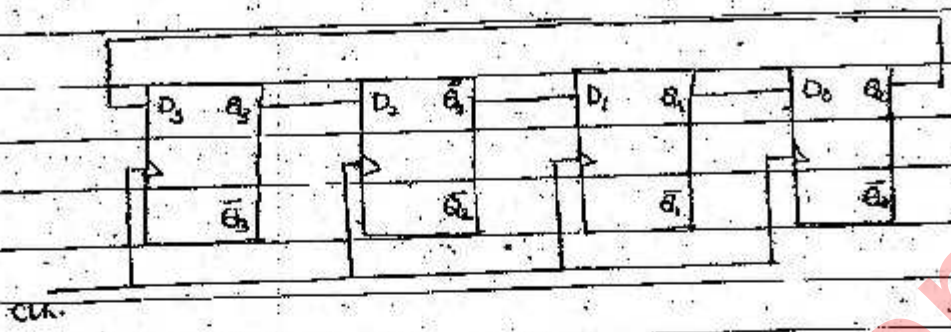
1. Trigger → +ive, -ive
2. Clock → Q, $\bar{Q}$
3. counter → UP, Down.
4. Preset /clear → clear → 000, Preset → 111
5. Decoding logic (Terminating logic)



dissmute

(c) Ring counter :- (Synchronous counter)

⇒ The last ff o/p is connected to first ff I/P.




(i) Explanation:-

⇒ Only one ff o/p is high and remaining FF are low.

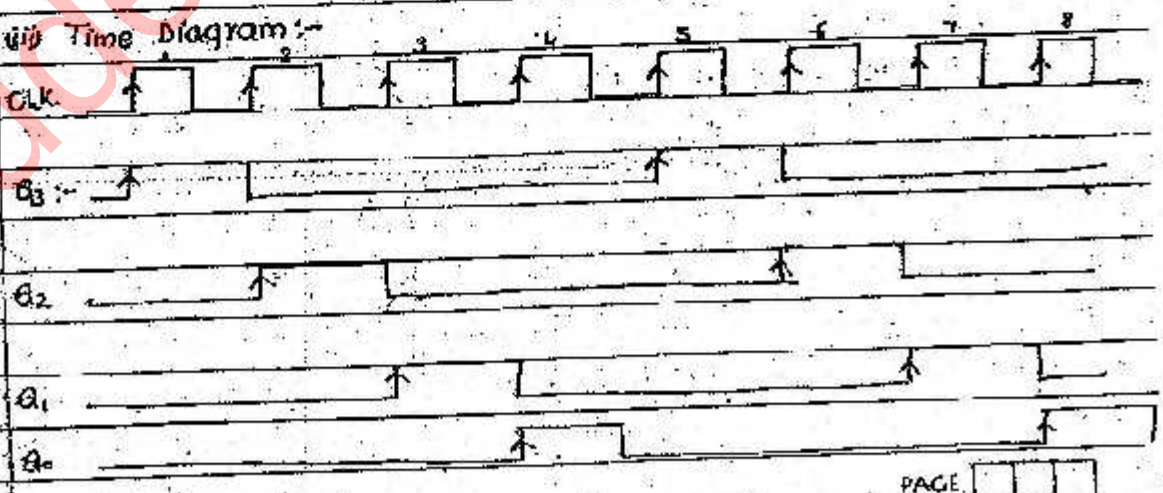
⇒ In 4 bit ring counter 4 states are there. (i.e. For n FF there is n states).

(ii) Truth table :-

| CLK | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | |
| 1 | 1 | 0 | 0 | 0 | 4-state |
| 2 | 0 | 1 | 0 | 0 | |
| 3 | 0 | 0 | 1 | 0 | |
| 4. | 0 | 0 | 0 | 1 | |
| 5. | 1 | 0 | 0 | 0 | |

⇒ In synchronous counter the +ive edge or -ive edge, the o/p remains same.

(iii) Time Diagram :-

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⇒ n bit ⇒ n state

⇒ $f_0 = f/n$

⇒ Phase shift b/w generated waveform is $360/n$.

$$\phi = \frac{360}{n}$$

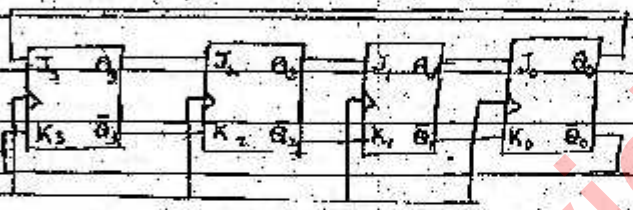
Application :-

⇒ used in stepper motor control.

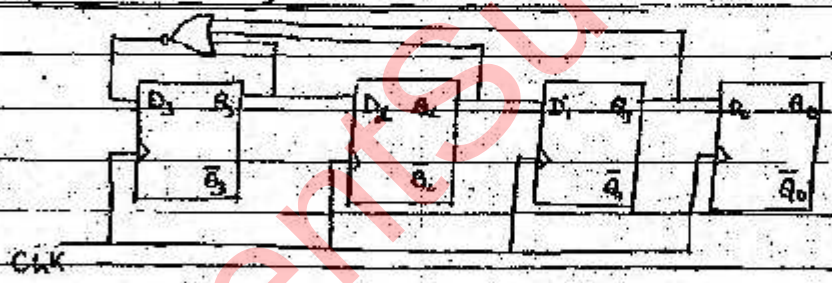
⇒ in Analog to Digital converter

⇒ No. of unused state in ring counter is $2^n - n$.

ring counter using J-K :-




* self starting Ring counter :-




⇒ Advantage of Ring counter is decoding is simple. to decode no logic gate are required.

⇒ last o/p can not be connected in the I/P of self start ring counter.



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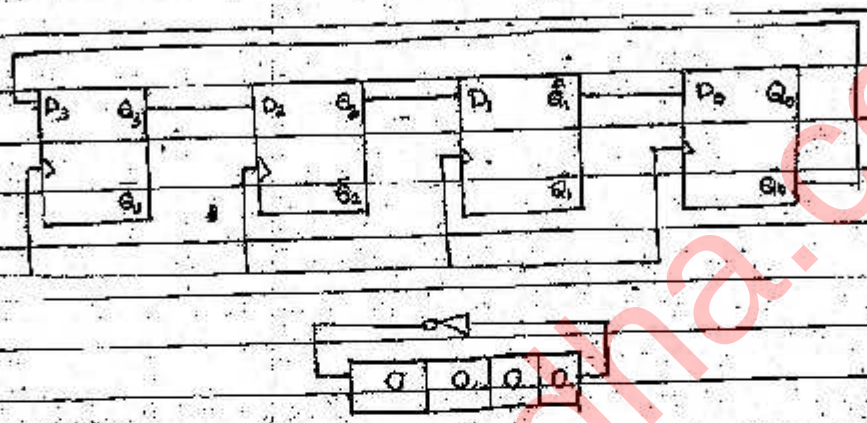
## (D) Johnson Counter :-

⇒ Symmetric o/p waveform.

⇒ 8-stages are there for 4 bit counter.

⇒ phase shift = $\frac{360}{4}$ = 90°

⇒ It is just like SISO register.







(ii) Truth Table :-

| CLK | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |
| 8 | 0 | 0 | 0 | 0 |

8 state

⇒ Total no. of used state = 8

⇒ Total no. of unused state = $2^n - 8 = 2^4 - 8 = 8$ state.

⇒ Also called Twisted Ring counter, Mobies counter or, creeping counter or, Walking counter or, switch tail counter.

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| CLOCK | $Q_3$ $Q_2$ $Q_1$ $Q_0$ | | |
|---|---|---|---|
| 0 | 0 0 0 0 | → | $\bar{Q}_3 \bar{Q}_0$ |
| 1 | 1 0 0 0 | → | $Q_3 \bar{Q}_1$ |
| 2 | 1 1 0 0 | → | $Q_2 \bar{Q}_1$ |
| 3 | 1 1 1 0 | → | $Q_1 \bar{Q}_0$ |
| 4 | 1 1 1 1 | → | $Q_3 Q_0$ |
| 5 | 0 1 1 1 | → | $\bar{Q}_3 Q_2$ |
| 6 | 0 0 1 1 | → | $\bar{Q}_2 Q_1$ |
| 7 | 0 0 0 1 | → | $\bar{Q}_1 Q_0$ |
| 8 | 0 0 0 0 | | |

(A)

⇒ In Johnson counter to decode each state one two I/p. AND / NOR gate used.

Disadvantage:

⇒ lock out may occur. (when counter enter into unused state)

Note:- In synchronous counter propagation delay of each counter is $t_{pdff}$ then.

$$T_{CLK} \geq t_{PDFF}$$

$$f_{CLK} \leq \frac{1}{t_{pdff}}$$

$$f_{max} = \frac{1}{t_{pdff}}$$

In synchronous counter.

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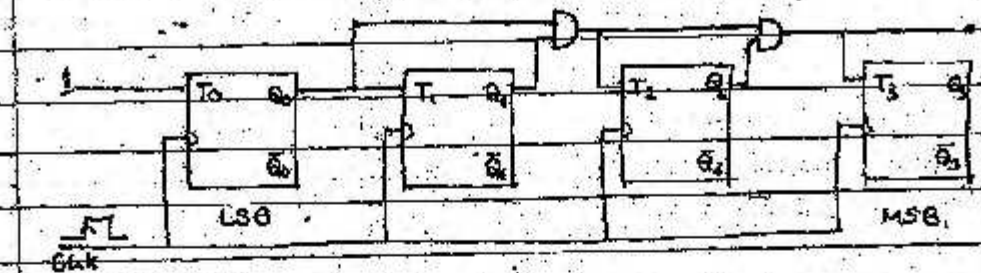
(A) Synchronous Series carry counter :-




(i) Explanation :-

⇒ ckt shown in fig. is Synchronous series carry up counter.

⇒ In this counter $Q_0$ toggles for every clock pulse.

⇒ $Q_1$ toggles when $Q_0 = 1$ and clock is applied.

⇒ $Q_2$ toggles when $Q_1 = Q_0 = 1$ and clock applied

⇒ $Q_3$ will toggles when $Q_2 = Q_1 = Q_0 = 1$ and clock applied.

⇒ This ckt may be down counter when $\bar{Q}$ is connected to T.

(ii) Truth table :-

| Clock | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |

⇒ To provide down counter used $\bar{Q}$ o/p to provide next stage I/p.

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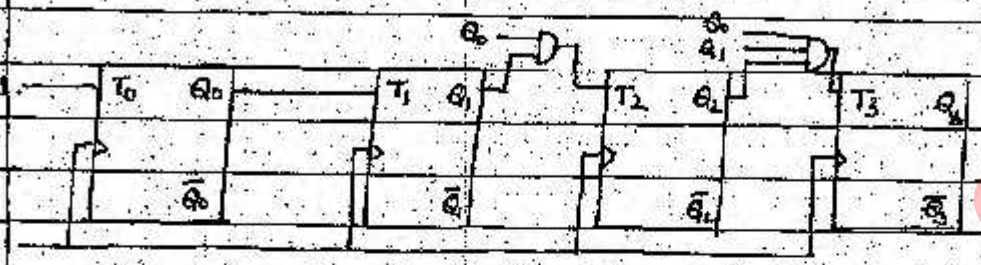
$$T_{CLK} \geq t_{PdFF} + (n-2)\, t_{PdAND}$$

(B) Synchronous parallel carry counter :-




⇒ Faster than series carry counter.

⇒ Disadvantage is increased I/P pin of AND Gate.

$$T_{CLK} \geq t_{PdFF} + t_{PdAND}$$

⇒ Sync

⇒ Ripple counter < Synchronous serial carry < Synchronous parallel carry counter for faster logic.

Problem:

Sol:

Sol:

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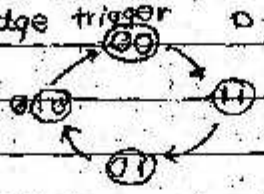
## Synchronous counter design for the given sequence :-

Problem:- Design a synchronous counter for the count sequence 0→3→1→2→0

Sol:- using +ve edge trigger D-FF.



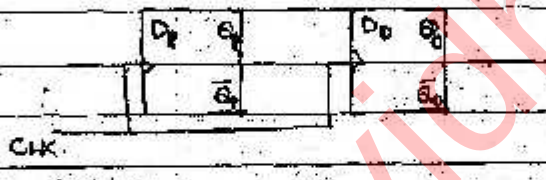

STATE DIAGRAM

Sol:- Procedure :-

(i) Identify no. of FF and I/P and O/P.
(ii) construct state table.
(iii) logical expression for I/P.
(iv) Minimize.
(v) Implement the ckt.

Now,

(i)




(ii) state table :-

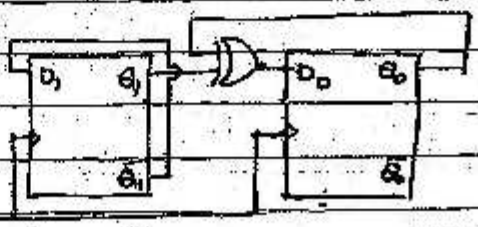
| Present state | | Next state | | | |
|---|---|---|---|---|---|
| $Q_1$ | $Q_0$ | $Q_{1+}$ | $Q_{0+}$ | $D_1$ | $D_0$ |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |

(iii) logical expression :-

$D_1 = \bar{Q}_1\bar{Q}_0 + \bar{Q}_1 Q_0 = \bar{Q}_1 (Q_0 + \bar{Q}_0) = \bar{Q}_1$

$D_0 = \bar{Q}_1\bar{Q}_0 + Q_1 Q_0 = Q_1 \oplus Q_0 = Q_1 \odot Q_0$

(iv) Implementation :-

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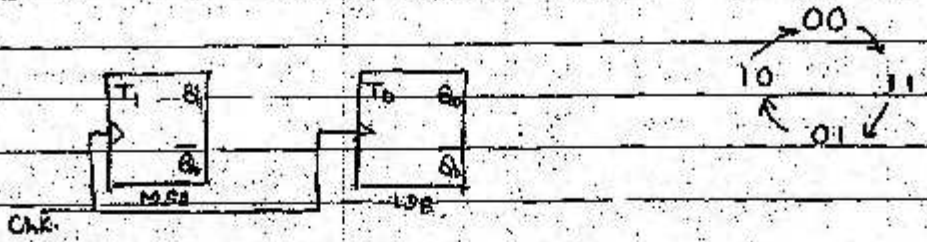
Q: Design using T-FF. 0-3-2-1-2-0.

Sol:- (i)




(ii) State table.

| $Q_1$ | $Q_0$ | $Q_{1+}$ | $Q_{0+}$ | $T_1$ | $T_0$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |

(iii) logical expression:

$T_1 = 1$

$T_0 = \bar{Q}_1\bar{Q}_0 + \bar{Q}_1 Q_0 = \bar{Q}_1$

(iv) Implementation:-

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Content :-

⇒ Various no. system.

⇒ Arithmetic operation → complement
→ Add, sub.

⇒ Various codes.

⇒ Data representation → unsigned
→ signed → signed magnitude
→ 1's
→ 2's

Number system and codes :-

| Weighted | Unweighted |
|---|---|
| ⇒ Positional weighted | ⇒ No weighted |
| e.g. Binary, octal | e.g. gray code, Excess-3 coc |
| Decimal, Hexdecimal | |
| BCD code. | |

⇒ A number system with base or radix r contains, r different digit and they are from (0 — r-1).

e.g. $(101)_r$

r = Base or radix.

| Base | Different Digit |
|---|---|
| 2 | 0, 1 |
| 8 | 0, --- 7 |
| 10 | 0, --- 9 |
| 12 | 0, --- 9, A, B |
| 16 | 0, 9, A, B, C, D, E, F |
| 4 | 0, --- 3 |
| 6 | 0, 1, 2, 3, 4, 5 |

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☆ Conversion (various number System) :-

1. Decimal to others :-

⇒ To convert decimal no. into any other base r divide integer part multiply fractional part with r.

e.g.

Q:- Convert $(25.625)_{10}$ — $(\quad)_2$.

Sol:-

| | | |
|---|---|---|
| 2 \| 25 | | |
| 2 \| 12 | – 1 | ↑ |
| 2 \| 6 | – 0 | |
| 2 \| 3 | – 0 | |
| 2 \| 1 | – 1 | |
| 0 | – 1 | |

$0.625 \times 2 = 1.25 = 1.$ ↓

$0.25 \times 2 = 0.50 = 0$

$0.5 \times 2 = 1.0 = 1$

Ans :- $(11001.101)_2$

Q:- Convert $(25.625)$ — $(\quad)_8$

Sol:-

| | | |
|---|---|---|
| 8 \| 25 | | |
| 8 \| 3 | – 1 | ↑ |
| 0 | – 3 | |

$0.625 \times 8 = 5$

Ans :- $(31.5)_8$.

⇒ When we go from higher to lower base the no. it is increased.

Q:- Convert $(25.625)_{10}$ – $(\quad)_{16}$

Sol:-

| | | |
|---|---|---|
| 16 \| 25 | | |
| 16 \| 1 | – 9 | ↑ |
| 0 | – 1 | |

$0.625 \times 16 = 10. = A$

Ans :- $(19.A)_{16}$.

Q:- Convert $(254)_{16}$ – $(\quad)_4$.

Sol:-

| | | |
|---|---|---|
| 16 \| 254 | | |
| 16 \| 15 | 14 = E | ↑ |
| 0 | 15 = F | |

$= (FE)_{16}$



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Q: Convert $(27.4)_{10} = (\_)_4$

Sol:

| | | |
|---|---|---|
| 4 \| 27 | | |
| 4 \| 6 – 3 ↑ | $0.4 \times 4 = 1.6 = 1$ | ↓ |
| 4 \| 1 – 2 | $0.6 \times 4 = 2.4 = 2$ | |
| 0 – 1 | $0.4 \times 4 = 1.6 = 1$ | |

Ans :- $(123.\overline{12})_4$

2. Others to Decimal :-

$(X_1 X_2 X_3 . Y_1 Y_2)_r = (\quad)_{10}$

⇒ To convert any other base r to decimal multiply each digit with positional weighted then add.

then,

$(\_)_{10} = X_1 \times r^2 + X_2 r^1 + X_3 \times r^0 + Y_1 r^{-1} + Y_2 r^{-2}$

Q: Convert $(10101.11)_2 = (\_)_{10}$.

Sol: $1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2}$

$= 16 + 4 + 1 + 1/2 + 1/4$

$= \frac{64+16+4+2+1}{4} = \frac{87}{4} = (21.75)_{10}$

Q: Convert $(57.4)_8 = (\quad)_{10}$.

Sol: $5 \times 8^1 + 7 \times 8^0 + 4 \times 8^{-1}$

$= 40 + 7 + \frac{4}{8} = \frac{320+56+4}{8} = \frac{380}{8}$

$= 47.5 = (47.5)_{10}$

Q: Convert $(57.4)_{16} = (\quad)_{10}$

Sol: $5 \times 16 + 7 + \frac{4}{16} = 87 + 0.25 = (87.25)_{10}$

Q: Convert $(BAD)_{16} = (\quad)_{16}$

Sol: $11 \times 16^2 + 10 \times 16 + 13$

$= 256 \times 11 + 160 + 13$

$= 2816 + 160 + 13 = (2989)_{10}$.

DATE

Q:- convert $(35)_6 = (-)_{10}$

Sol:- $3\times6 + 5\times1 = 18+5 = (23)_{10}$

3. Octal to Binary & Binary to Octal :-

$(xyz)_8 = (-)_2$

⇒ each no. is represent by its 3 bit binary formate.

Ques:- convert $(37.45)_8 = (\ )_2$

Sol:- $(011\,111 . 100\,101)_2$

Binary to octal :-

Ques:- convert $(110\,110 . 11)_2$

Sol:- $(010\,110 . 110)_2$

$= (26.6)_8$

4. Hexadecimal to Binary and Binary to Hexadecimal :-

⇒ Each digit is represent by 4 bit binary.

Ques:- convert $(259A)_{16} = (-)_2$

Sol:- $(0010\,0101\,1001\,1010)_2$

5. Hexadecimal to octal or octal to Hexa :-

for Hexa ⟷ Octadecimal

Hexa ④→ Binary ←③ Octadecimal

Q:- convert $(CAD)_{16} = (\ )_8$

Sol:- $(CAD)_{16}$

$= (1100\,1010\,1101)_2$

$= (6255)_8$