BOOLEAN ALGEBRA

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⇒ Boolean Algebra :-

(i) when no. of variable are less (1,2,3)

(ii) It is preffered when output is 0 or 1.

⇒ K-map :-

(i) When no. of variables are 2,3,4,5 (upto 5 variable)

(ii) output is 0, 1 or, x.

⇒ Tabulation method.

(i) It is used when no. of variables are more.

Boolean Algebra :-

⇒ A complement → $\bar{A}$ or, A'

$\bar{\bar{A}} = A$

⇒ NOT :-

$\bar{0} = 1$

$\bar{1} = 0$

⇒ AND :-

$0 \cdot 0 = 0$	$A \cdot A = A$
$0 \cdot 1 = 0$	$A \cdot 1 = A$
$1 \cdot 0 = 0$	$A \cdot 0 = 0$
$1 \cdot 1 = 1$	$A \cdot \bar{A} = 0$

⇒ OR :-

$0+0 = 0$	$A+A = A$
$0+1 = 1$	$A+1 = 1$
$1+0 = 1$	$A+0 = A$
$1+1 = 1$	$A+\bar{A} = 1$

Problem:- $AB + A\bar{B}$

Sol:- $A(B+\bar{B})$ $\quad (\because B+\bar{B} = 1)$

$= A$

Problem:- $AB + A\bar{B}C + A\bar{B}\bar{C}$, find the min. no. of NAND Gate.

option. ✓(a) 0 (b) 1

(c) 2 (d) 3

Sol^n:- $AB + A\bar{B}C + A\bar{B}\bar{C}$

$= AB + A\bar{B}(C+\bar{C})$

$= AB + A\bar{B}$ $\quad (\because C+\bar{C} = 1)$

$= A(\bar{B}+B)$

$= A$

No NAND gate required. $\quad A \xrightarrow[\text{i/p} \qquad \text{o/p}]{} A$

Advantage of Minimization :-

⇒ No. of logic gate ↓

⇒ speed ↑.

⇒ Power dissipation ↓

⇒ complexity of circuit less.

⇒ fan in ↓ — (no. of input ↓)

⇒ cost ↓.

Problem:- Simplify :-

(a) $A\bar{B} + AB\bar{C} + A\bar{B}\bar{C}D$

Sol^n:- $A\bar{B}\bar{C} + A\bar{B}(1+\bar{C}D)$

$= AB\bar{C} + A\bar{B}$ $\quad (1+x = 1)$

$= A(\bar{B}+B\bar{C})$ $\quad (\because \bar{B}+B\bar{C} = \bar{B}+\bar{C})$

$= A(\bar{B}+\bar{C})$

$= A\bar{B} + A\bar{C}$

(b) $(A+B)(A+C)$

Sol^n:- $A.A + AC + AB + BC$

$= A + A(1+B) + BC$

$= A(1+B+C) + BC$

$= A + BC$

Transposition Theorem

$$\boxed{(A+B)(A+C) = A + BC}$$

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Similarly:

$$\boxed{(\bar{X}+Y)(\bar{X}+Z) = \bar{X}+YZ}$$

(c) $(A+B+C)(A+\bar{B}+C)(A+B+\bar{C})$

Sol:- take $A+B = X$

$= (X+C)(A+\bar{B}+C)(X+\bar{C})$

$= (X+C\bar{C})(A+\bar{B}+C)$

$= X(A+\bar{B}+C)$

$= (A+B)(A+\bar{B}+C)$

$= A+B(\bar{B}+C)$

$= A+B\bar{B}+BC$

$= A+BC$

(d) $(A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})$

Sol:- $(A+B)(A+\bar{B})\quad(\bar{A}+B)(\bar{A}+\bar{B})$

$= (A+B\bar{B})(\bar{A}+B\bar{B})$

$= (A)(\bar{A})$

$= 0$

$\boxed{A+BC = (A+B)(A+C)}$ Distribution theorem

(e) $A+\bar{A}B$

Sol:- $(A+\bar{A})(A+B)$

$= 1(A+B) = A+B$

(f) $A+\bar{A}\bar{B}$

Sol: $(A+\bar{A})(A+\bar{B})$

$= 1(A+\bar{B}) = A+\bar{B}$

(g) $AB+\bar{A}\bar{B}+A\bar{B}$

Sol: $A(B+\bar{B})+\bar{A}\bar{B}$

$= A+\bar{A}\bar{B}$

$= (A+\bar{A})(A+\bar{B})$

$= A+\bar{B}$ Ans.

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(h) $AB + \bar{A}B + A\bar{B}$

Sol^n:- $B(A+\bar{A}) + A\bar{B}$

$= B + A\bar{B}$

$= (B+A)(B+\bar{B})$

$= A+B$ Ans.

(i) $AB\bar{C} + ABC + \bar{A}BC$

Sol^n:- $AB\bar{C} + ABC + ABC + \bar{A}BC$ $(\because A+A = A)$

$= AB(C+\bar{C}) + (A+\bar{A})BC$

$= AB + BC$

$= B(A+C)$

(j) $AB + \bar{A}C + (BC)$ ——→ redundant term.

Sol^n:- $AB + \bar{A}C + BC(A+\bar{A})$

$= AB + \bar{A}C + BCA + \bar{A}BC$

$= AB(1+C) + \bar{A}C(1+B)$

$= AB + \bar{A}C$

Note:- In this case BC is known as redundant term i.e. not used or not compulsory term.

⇒ $AB + \bar{A}C + BC = AB + \bar{A}C$, called consensus theorem or redundancy theorem.

⇒ Shortcut method :-

(a) Three variable

(b) each variable comes twice.

(c) one variable is complemented.

(k) $AB + B\bar{C} + AC$

Sol^n:- $B\bar{C} + AC$ { The term which is complemented is taken.

(l) $A\bar{B} + BC + AC$

Sol^n:- $A\bar{B} + BC$

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(m) $(\bar{A}+B)(\bar{A}+C)(B+C)$

Sol:- $(A+B)(\bar{A}+C)$ $\because (B+C)$ is redundant term.

(n) $(A+B)(\bar{B}+C)(A+C)$

Sol:- $(A+B)(\bar{B}+C)$

(o) $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C}$

Sol:- In this case all the variable are complemented only one are uncomplemented then.

$= \bar{A}\bar{B} + A\bar{C}$ ($\because$ The term which is uncomplemented is taken)

(p) $\bar{A}\bar{B} + \bar{B}C + \bar{A}\bar{C}$

Sol:- $\bar{B}C + \cancel{\bar{A}\bar{B}}\ \bar{A}\bar{C}$

(q) $(\bar{A}+B)(\bar{B}+\bar{C})(\bar{A}+\bar{C})$

Sol:- $(\bar{B}+\bar{C})(\bar{A}+C)$

$$\boxed{\begin{array}{l} \overline{ABC} = \bar{A}+\bar{B}+\bar{C} \\ \overline{A+B+C} = \bar{A}\cdot\bar{B}\cdot\bar{C} \end{array}}$$ Demorgan's theorem.

Boolean Algebra :-

↳ Minimization

⇒ SOP → minimal, canonical

⇒ POS → minimal, canonical

⇒ Dual

⇒ Complement Expression

⇒ Truth table

⇒ Venn Diagram

⇒ Switching circuit

⇒ Statement

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(A) **Minimization :-**

(a) $XY + \overline{XY}WZ$

Sol^n: $A = XY$ and $B = WZ$

Then,

$= A + \bar{A}B$

$= (A+\bar{A})(A+B)$

$= A+B$

$= XY + WZ$

(b) let $f(A,B) = \bar{A} + B$ Then, the value of $f[f(x+y, y), z)$ is

(a) $xy + z$ (c) $\bar{x}y + z$

(b) $x\bar{y} + z$ (d) x

Sol^n:- $f[f\{(x+y), y\}, z]$

$= F[\overline{x+y} + y, z]$

$= F[\bar{x}.\bar{y} + y, z]$

$= \overline{\bar{x}\bar{y} + y} + z$

$= \overline{\bar{x}\bar{y}} . \bar{y} + z$

$= (\bar{\bar{x}} + \bar{\bar{y}})\bar{y} + z$

$= x\bar{y} + y\bar{y} + z$

$= x\bar{y} + z$ Ans.

(c) let $x * y = \bar{x} + y$ and $z = x * y$

Then the value of $z * x$ is

(a) x (c) 0

(b) 1 (d) $\bar{x}$

(B) SOP (Sum of Product Form)

$\underline{ABC} + \underline{\bar{A}BC} + \underline{AB\bar{C}}$
↳ minterm

⇒ In SOP form, each product term is known as Minterm or Implicant

⇒ Sop Form is used when O/P of logical expression is 1.
(means $1 \rightarrow A$ and $0 \rightarrow \bar{A}$)

Ex :- $5 \rightarrow 101 \rightarrow A\bar{B}C$

$9 \rightarrow 1001 \rightarrow A\bar{B}\bar{C}D$

Ques:- For the given truth table, minimize SOP expression.

	A	B	Y
$\bar{A}\bar{B}$	0	0	1 ⇐
	0	1	0
$A\bar{B}$	1	0	1 ⇐
	1	1	0

Sol:- In SOP form only 1 taken.

$= \bar{A}\bar{B} + A\bar{B}$

$= \bar{B}(\bar{A}+A)$

$= \bar{B}$

⇒ Y can written as :-

$Y(A,B) = \Sigma m(0,2)$

Ques:- Simplified the expression for

$Y(A,B) = \Sigma m(0,2,3)$

Sol:- 00 10 11

logical expression in sop form :-

$Y = \bar{A}\bar{B} + A\bar{B} + AB$

$= \bar{B}(\bar{A}+A) + AB$

$= \bar{B} + AB$

$= (\bar{B}+A)(\bar{B}+B)$

$= A+\bar{B}$

$= A+\bar{B}$

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SOP can be of two form-

(1) Minimal form

(2) Canonical form.

$\Rightarrow$ $A + \bar{A}B = A + B$ (It is a minimal form)

$\Rightarrow$ In canonical form, each term must have all variable.

e.g. $A + \bar{A}B$

$= A(B+\bar{B}) + \bar{A}B$

$= AB + A\bar{B} + \bar{A}B$

Thus each min term will contain all variable.

IES-2003

Problem:- In canonical (SOP form), no. of min term presenting the logical expression $A + \bar{B}C$ is.

(a) 4 (c) 6

✓ (b) 5 (d) 7

Sol^n:-

$A + \bar{B}C$

$= A(B+\bar{B})(C+\bar{C}) + \bar{B}C(A+\bar{A})$

$= (AB + A\bar{B})(C+\bar{C}) + A\bar{B}C + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$

i.e. 5 terms.

(C) POS Form (Product of Sum) :-

$(A+B+\bar{C})\ (\bar{A}+B+C)\ (A+B+C)$

↳ max term

⇒ POS form are used when o/p is logic '0'.

$0 \rightarrow A$

$1 \rightarrow \bar{A}$

Ex :- $5 \rightarrow 101 \rightarrow \bar{A}B\bar{C}$

$9 \rightarrow 1001 \rightarrow \bar{A}BC\bar{D}$

Ques:- For a given ~~th~~ truth table minimize POS expression.

	A	B	Y
	0	0	1
$A+\bar{B}$	0	1	0
	1	0	1
$\bar{A}+\bar{B}$	1	1	0

Sol:- we take only that value at which o/p is '0'.

$Y = (A+\bar{B})\ (\bar{A}+\bar{B})$

$= \bar{B} + A\bar{A}$

$= \bar{B}$

⇒ Y can be written in POS form as,

$Y(A,B) = \prod M(1,3) = \bar{B}$

and for SOP :-

$Y(A,B) = \sum m(0,2) = \bar{B}$

i.e.

$\sum m(0,2) = \prod M(1,3)$

⇒ If $F(A,B,C) = \sum m(0,1,4,7)$

There are 3 variable then 8 combination then max-term are, 2,3,5,6.

$F(A,B,C) = \sum m(0,1,4,7) = \prod M(2,3,5,6)$

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⇒ with 'n' variable, maximum possible minterms or maxterms are 2^n. eg.

(i) for, $n = 2$. i.e. (A, B)

∴ Total no. of min or max terms are $2^2 = 4$.

(ii) for, $n = 3$ i.e. (A, B, C)

Total no. of min or max terms are $2^3 = 8$.

⇒ For $n = 2$, (A, B) total 16 logical expression i.e.

1	A	$A\bar{B}$	AB
0	$\bar{A}$	$\bar{A}B$	$A+B$
$\bar{A}B + A\bar{B}$	B	$A+\bar{B}$	$\bar{A}\bar{B}$
$AB + \bar{A}\bar{B}$	$\bar{B}$	$\bar{A}+B$	$\bar{A}+\bar{B}$

Note :- With n variable maximum possible logical expression are 2^{2^n}.

eg. for $n = 2$, logical expression $= 2^{2^2} = 16$

for $n = 3$ $= 2^{2^3} = 256$

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GATE-2003
ITO-2001
ITO-2002

Problem:- For $n = 4$ what is the total no. of logical expression.

Sol^n:- logical expression $= 2^{2^4}$

$= 2^{16} = 35536.$

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(D) Dual form :-

+ive logic	-ive logic
⇒ +ive logic means higher voltage corresponds to logic '1'.	⇒ -ive logic means higher voltage corresponds to logic '0'.
⇒ logic '0' → 0 V, logic '1' → +5V	⇒ logic 0 = +5V, logic 1 = 0V.

Ques:- logic 0 → -5V
logic 1 → 0V

Sol^n:- Higher value of voltage (0V) for logic 1. then +ive logic.

Ques:- ECL :
logic '0' → -1.7V
logic 1 → -0.8V

Sol^n:- -0.8V is larger value than -1.7V then it is +ive logic.

+ive logic AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

-ive logic AND

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

+ive logic OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

-ive logic OR

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

⇒ For -ive logic or gate, convert 1 to 0 and 0 to 1.

⇒ We can say that +ive logic AND gate is equal to -ive logic OR gate and -ive logic AND gate is equal to +ive logic OR gate.

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⇒ Dual expression is used to convert +ive logic into -ive logic or, -ive logic to +ive logic.

⇒ $AB \xrightarrow{\text{Dual}} A+B$

∴ Dual is nothing but -ive logic.

⇒ AND $\xrightarrow[\text{Dual}]{\text{-ive logic}}$ OR

⇒ OR $\xrightarrow[\text{Dual}]{\text{-ive logic}}$ AND

(-) AND ⟷ OR
(-) $\cdot$ ⟷ $+$
(-) 1 ⟷ 0
(-) keep variable as it is

} Dual.

Problem: Find Dual.

$AB\bar{C} + \bar{A}BC + ABC$

Sol:- Dual :-

$(A+B+\bar{C})(\bar{A}+B+C)(A+B+C)$

if we find again dual then,

$AB\bar{C} + \bar{A}BC + ABC$

⇒ For any logical expression, if two times dual is used resulting same expression.

Self Dual :-

$AB + BC + AC$

Dual :-

$= (A+B)(B+C)(A+C)$

$= (B+AC)(A+C)$

$= BA + BC + AC + AC$

$= AB + BC + AC$ (again same expression)

⇒ In some of the logical expression not all its dual gives the same expression.

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⇒ In self Dual expression, if one time dual is used result in same expression.

$$\boxed{n \text{ variable} \rightarrow \text{self Dual} = 2^{2^{n-1}}}$$

i.e. If there are n variables then total no. of self dual expression is $2^{2^{n-1}}$.

eg :-

(i) For $n = 1$. ⇒ $2^{2^0} = 2$.

Then 2 dual expression.

$A \rightarrow$ Self dual $\rightarrow A$

$\bar{A} \rightarrow \bar{A}$

Total self dual expression are 2.

(ii) For $n = 2$ ⇒ $2^{2^1} = 4$.

Then 4 dual expression.

$A \rightarrow A$, $B \rightarrow B$

$\bar{A} \rightarrow \bar{A}$, $\bar{B} \rightarrow \bar{B}$

(iii) For $n = 3$ ⇒ $2^{2^{3-1}} = 16$.

Then 16 dual expression.

$A, \bar{A}, B, \bar{B}, C, \bar{C}, \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$, $AB + BC + CA$, ...

(E) Complement :-

if $Y = ABC + \bar{A}BC + A\bar{B}C$

complement is,

$\bar{Y} = (\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})$

(i) AND ⟷ OR

(i) $\cdot$ ⟷ $+$

(i) 1 ⟷ 0

(i) complement of each variable.

complement.

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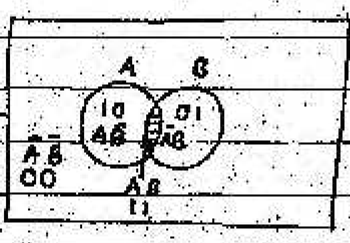
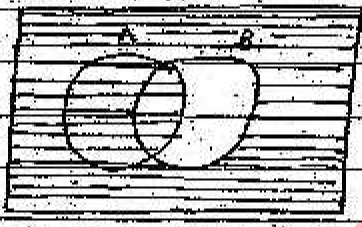
(F) Venn Diagram :-

For two variable (A, B).



Ques :- For a given venn diagram, minimize the SOP expression for shaded region.



Sol :-

$$Y = \bar{A}\bar{B} + A\bar{B} + AB$$
$$= \bar{B}(\bar{A} + A) + AB$$
$$= \bar{B} + AB$$
$$= (\bar{B} + A)(\bar{B} + B)$$
$$= A + \bar{B}$$

(0 1) for POS form.

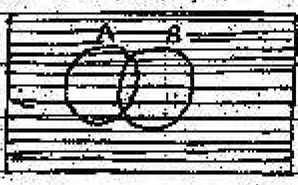
Ques :- SOP expression for shaded region.

Sol :-

$$Y = AB + A\bar{B} + \bar{A}B$$
$$= A(B + \bar{B}) + \bar{A}B$$
$$= A + \bar{A}B$$
$$= (A + \bar{A})(A + B)$$
$$= A + B$$

$(0, 0) \longrightarrow$ (in POS form)

Ques :- SOP expression



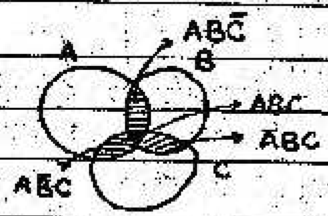
Sol:- $\bar{A}B + A\bar{B} + AB + \bar{A}\bar{B}$

$= B(A+\bar{A}) + \bar{B}(A+\bar{A})$

$= B + \bar{B}$

$= 1.$

$\Rightarrow$ For 3- variable :-



SOP form for shaded portion

$= ABC + \bar{A}BC + AB\bar{C} + A\bar{B}C + \underline{ABC + ABC}$ $\hookrightarrow$ extra added

$= BC(A+\bar{A}) + AB(\bar{C}+C) + AC(B+\bar{B})$

$= AB + BC + CA$

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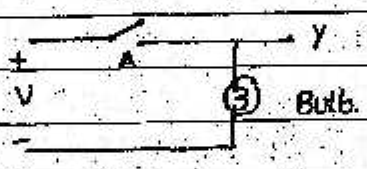
(6) Switching Circuit :-

For Series :-

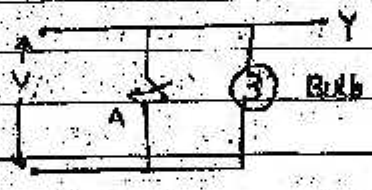
Truth table :-

A	Y
0	0
1	1



For Parallel :-

A	Y
0	1
1	0



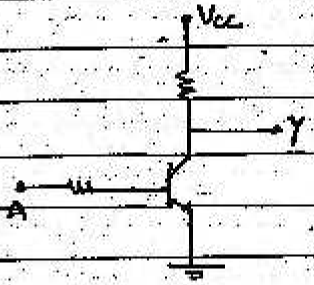
⇒ In place of bulb if there is resistor then answer remains the same but some drop.

Truth table :-

A	Y
0	1
1	0

⇒ In place of switch if there is a transistor.

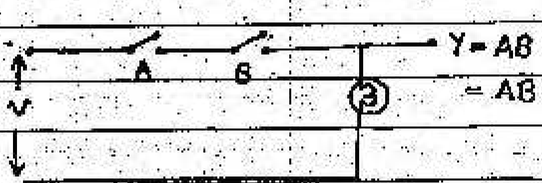
A	Y
0	1
1	0



(i) For A = 1 transistor becomes short circuit.

For two switch A and B :-

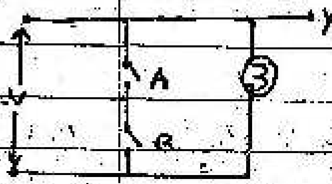
AND ⇒



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

alternate

NAND ⇒

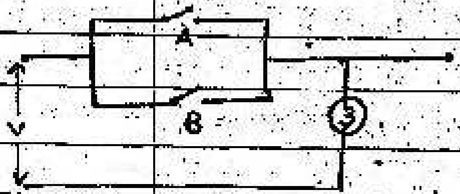


$Y = \overline{AB}$

$= \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

OR ⇒

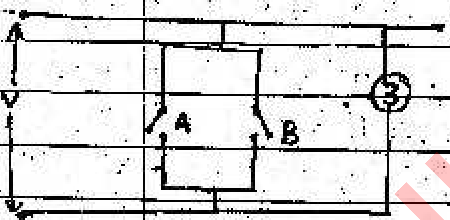


$Y = A+B$

$= A+B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOR ⇒



$Y = \overline{A+B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Ques:-

Sol:- $Y = A \cdot (B+C) \cdot \overline{D}$

$= (AB + AC)\overline{D}$

$= AB\overline{D} + AC\overline{D}$

(H). STATEMENT :-

(I)

Ques:- A logic circuit have 3 input A, B, C and o/p is Y.
o/p Y is 1 for the following combination.
(i) B and C are true $= BC$
(ii) A and C are false $= \bar{A}\bar{C}$
(iii) A, B and C are true $= ABC$
(iv) A, B and C are false $= \bar{A}\bar{B}\bar{C}$
then minimize the o/p for Y.

Sol:- o/p $Y = 1$. (take min term = SOP form)

$Y = BC + \bar{A}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$
$= BC(1 + A) + \bar{A}\bar{C}(1 + \bar{B})$
$= BC + \bar{A}\bar{C}$

if o/p $Y = 0$, then take max term (POS form).

Ques:- A logic ckt have 3 input A, B, C and o/p is $F = 1$ when majority no. of I/ps are logic 1. (IES Qu)
* (i) minimizing expression F
(ii) Implement logic ckt.

Sol:-

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$F = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$
$= \bar{A}BC + ABC + ABC + A\bar{B}C + AB\bar{C} + ABC$
$= BC(A + \bar{A}) + AC(B + \bar{B}) + AB(\bar{C} + C)$
$= AB + BC + CA$.

(I) LOGIC GATES :-

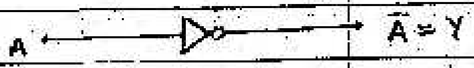
⇒ Basic Building Blocks

NOT, AND, OR } → Basic gate

NAND, NOR } → universal gate

EXOR, EXNOR } → Arithmetic ckt. comparator, parity generator/checker, code converters (Binary to gray, Gray to Binary)

NOT :-



A	Y
0	1
1	0

IES-2010 GATE-2010

Ques:- Circuit shown in the fig are

(a) Buffer
(b) Astable MV.
✓(c) Bistable MV
(d) square wave generator.

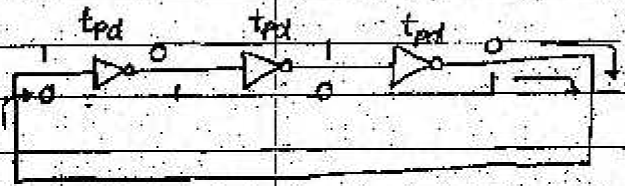
Sol:- If there is no feedback then it is buffer. In Buffer if we apply 0 then get 0
" 1 " " 1.
" no I/p " " no I/p.

Buffer means whatever the i/p ie. the o/p.

⇒ But there is a feedback and the o/p is stable if we give 1 as i/p, o/p is also 1 and if gives 0 then o/p is 0 then two stable state.

⇒ Hence it is a Bistable multivibrator.

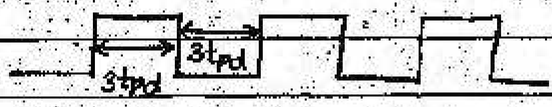
Ques:- Ckt shown is



Sol:- t_{pd} = Propogation delay

'0' for = $3 t_{pd}$

1 for = $3 t_{pd}$



It is called

(i) Square wave generator.

(ii) As o/p is not stable sometime 1 and sometime 0
Hence it is also called astable multivibrator.

(iii) clock generator

(iv) Ring oscillator.

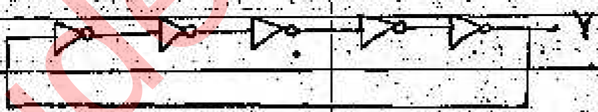
Total time period (T) = $6 T_{pd}$

then,

$$\boxed{T = 2N t_{pd}}$$

N = no. of inverters in feedback.

Ques:- In a ckt shown in fig. the propogation delay of each NOT gate is 100 P sec. then frequence of generator square wave is



(a) 10GHz
(b) 1GHz
(c) 100 MHz
(d) 10 MHz

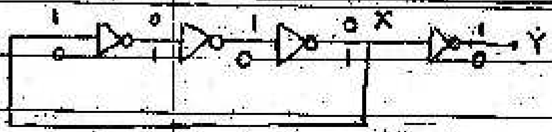
Sol:- $T = 2Nt_{pd}$

$= 2 \times 5 \times 100 \text{ Psec} = 1000 \text{ Psec}$

$f = \frac{1}{T} = \frac{1}{1000 \times 10^{-12} \text{ sec}} = 10^{9} \text{ Hz}$

alternate = 1GHz

Ques:



Sol^n: The ckt shown in the fig the propogation delay of each NOT gate is 2nsec. Then time period of generated square wave is.

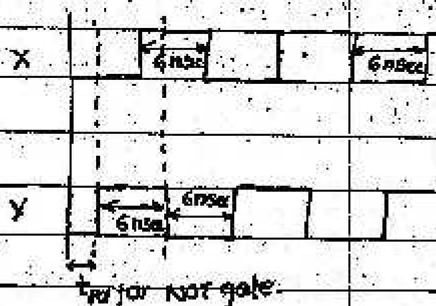
(a) 6ns (c) 14ns

(b) 12ns (d) 16ns

Sol:- Astable Multivibrator, square wave generator.

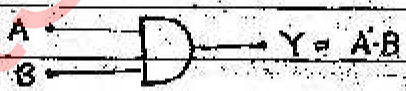
$T = 2 N t_{pd}$

$= 2 \times 3 \times 2 nsec = 12 nsec.$



Thus time period at x and y is same.

AND GATE :-



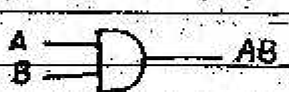
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

⇒ o/p is low if any of the I/p is low i.e logic '0'.

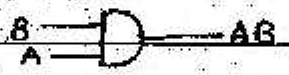
⇒ AND gate follow both commutative law and associative law.

(·) AB = BA

i.e.



or,



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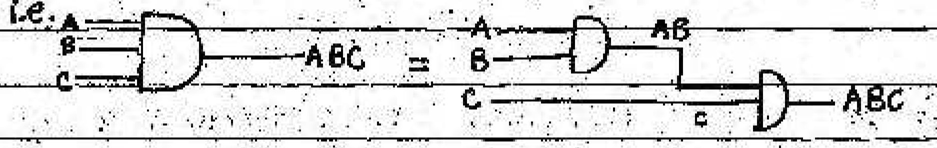
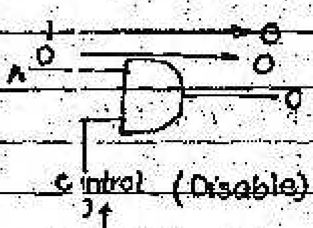
(i) ABC = (AB)·C = A.(BC)

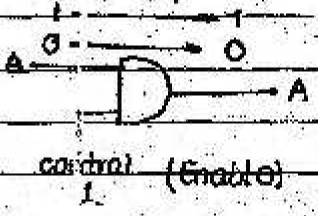
i.e.



⇒ Disable & Enables :-



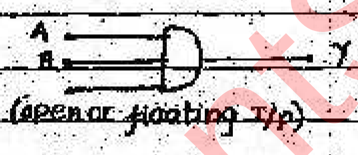
⇒ Thus O/P remains in '0' due to control I/P disable AND gate is not in working state.



⇒ AND gate is in working state, O/P is changing in Enabled state.

⇒ In TTL logic family, If any I/P is open and float then it will act as '1'.

⇒ In ECL logic family, floating input will act as logic '0'.



* Question occurs mostly from ECL and TTL in Exam.

Unused I/P's :-

1. 

⇒ In Multipin (I/P) AND gate unused I/p can be connected to logic 1. or "pull ~~off~~ up".

⇒ unused I/p can be connected to logic '0' or "pull Down".

alternate

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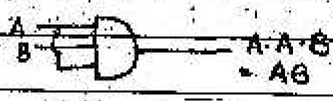
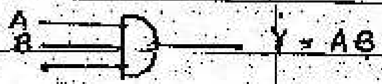
2. 



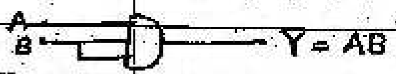
⇒ unused I/P can be connected to one of the used I/P.

3. 

(only for TTL)

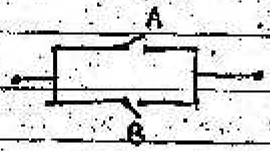
⇒ If it is TTL logic family, then unused I/P can be open or floated. (unconnected)

Note:- Because of unnecessary I/P attached to B, fan in will be down.



⇒ Best way to connecting unused pin (I/P) in AND gate is connecting to logic '1'.

OR Gate :- (Inclusive OR)



OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

⇒ When any of the I/P is High in OR gate then o/p is High.

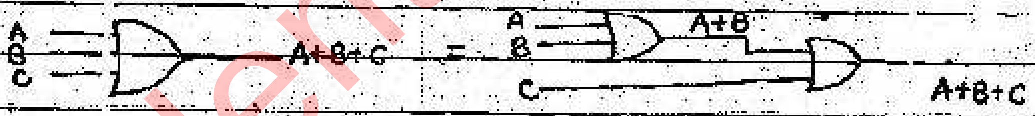
⇒ OR gate follows both commutative and Associative law.

(i) Commutative law :-

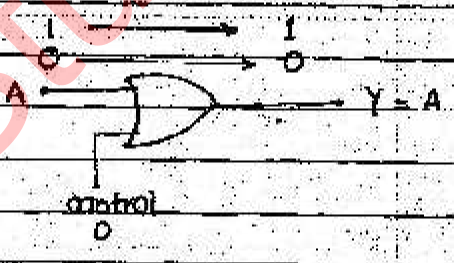
$A+B = B+A$

(ii) Associative law :-

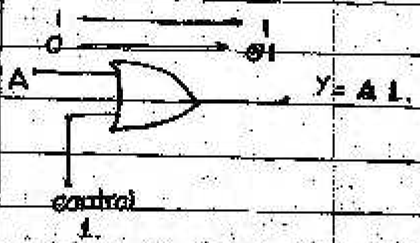
$A+B+C = (A+B)+C = A+(B+C)$



⇒ Enable and Disable :-



⇒ o/p is changing as I/P is changing or we say the gate is enabled.



⇒ o/p is fixed or not changed.
it is said to be disable.

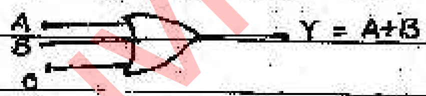
Unused I/p's :-

1. In OR gate, unused I/p is connected to logic '0' "pull down."

2. Connect to one of the used I/p.

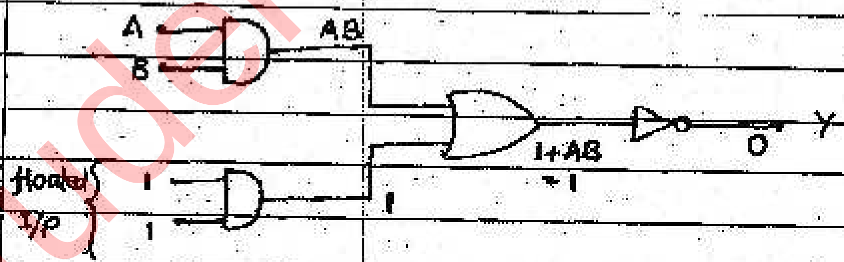
3. If it is ECL then unused I/p can be open or floated.

⇒ In OR gate, Best way of connecting the unused I/p is to connect to logic '0'.



Gate-2004.

Problem:- In the ckt shown in fig. in TTL, AND, OR, INVERTER ckt for the given I/p o/p is



(a) 0
(b) 1
(c) AB
(d) $\overline{AB}$

Sol:- In TTL, all I/p's are float then it is logic 1
alternate

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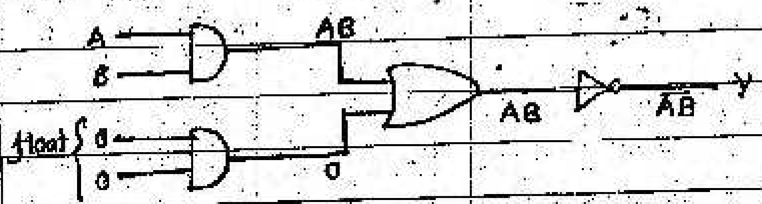
Problem: For ECL AND, OR, INVERTER.



(A) 0

(B) 1

(C) AB

(D) $\overline{AB}$

Sol^n:- If all I/P are floating in ECL then it is '0'

and o/p $Y = \overline{AB}$ Ans$_c$

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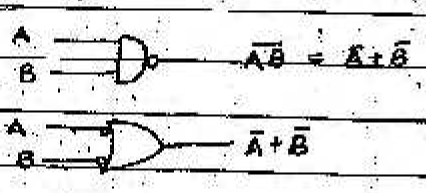
NAND GATE :- (Bubbled OR)



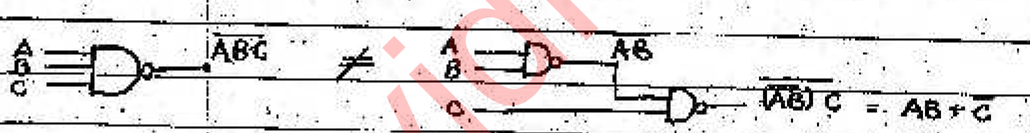
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

⇒ When both I/p high the O/p is low.

0 disable (not changing if one I/p is zero)

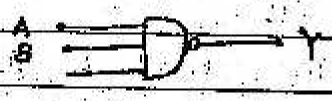
1 enable.

⇒ NAND gate follow commutative law but not follow associative law



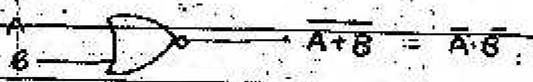
⇒ The only two gate not follow associative law i.e universal gate NAND or NOR gate.

⇒ Unused I/p in NAND gate can be connected similar to unused I/p in AND gate.



NOR GATE :- (Bubbled AND)

⇒ OR gate followed by NOT gate.



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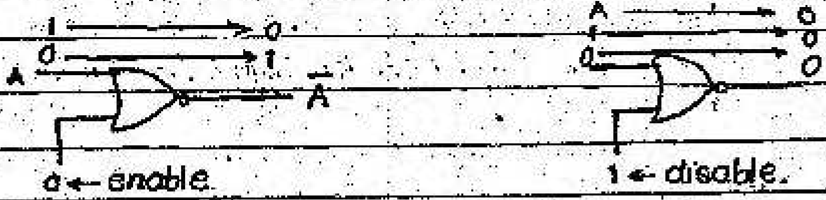
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

⇒ when both I/p is low the o/p is High.



⇒ enable and disable both are same as OR gate.

⇒ NOR gate follow commutative law and not follow associative law.

i.e. (i) $\overline{A+B} = \overline{B+A}$

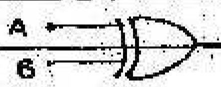
(ii) $\overline{A+B+C} \neq \overline{\overline{A+B}\ C}$

⇒ unused I/p in NOR gate can be connected similar to OR gate.

EXOR or, XOR :-

⇒ Exclusive OR gate.

⇒ OR gate is also called as inclusive OR gate.

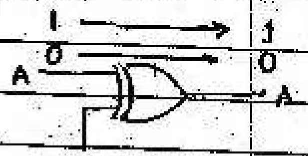


$Y = A \oplus B$

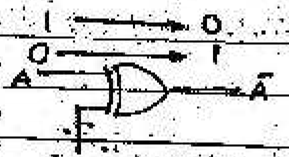
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

⇒ When A = B, o/p is low i.e '0'.

⇒ When A ≠ B, o/p is High i.e. logic '1'.



0 → Buffer



1 → inverter

⇒ It is also called controlled inverter.

Note :-
$A \oplus A = 0$
$A \oplus \bar{A} = 1$
$A \oplus 0 = A$
$A \oplus 1 = \bar{A}$

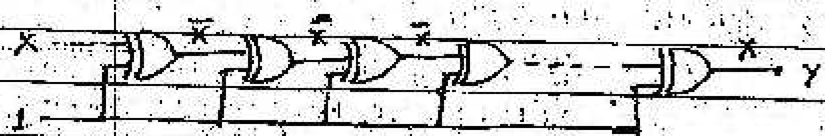
⇒ If $A \oplus B = C$ then,
(i) $A \oplus C = B$
(ii) $B \oplus C = A$
(iii) $A \oplus B \oplus C = 0$

⇒ Since, $A \oplus A = 0$
$A \oplus A \oplus A = A$
$A \oplus A \oplus A \oplus A = 0$
and so on - -

Then we say, odd no. of same I/P gives same O/P. and even no. same I/P gives zero as O/P.

⇒ $B \oplus B \oplus B \oplus \cdots n = B$; if n is odd.
$= 0$; if n is even.

Problem:- The ckt shown in fig. contains cascading of 20 EXOR gate. If X is the I/P then O/P is.
(a) 0
(b) 1
(c) X
(d) $\bar{X}$



Sol: O/P of even EXOR gate have same O/P.
$= X$ Ans. C

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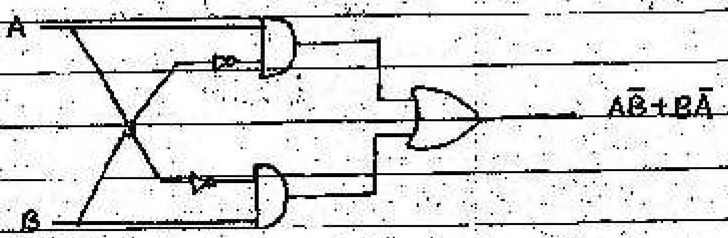
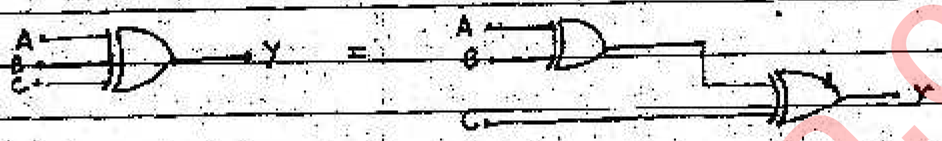
Internal diagram of EXOR gate :-



⇒ EXOR gate follow both commutative and associative law.

⇒ EXOR gate is ~~follow~~ available with two I/p's only.



Truth table :-

	A	B	C	Y $(A\oplus B\oplus C)$
	0	0	0	0
→	0	0	1	1
→	0	1	0	1
	0	1	1	0
→	1	0	0	1
	1	0	1	0
	1	1	0	0
→	1	1	1	1

⇒ The O/P of EXOR gate is 1 when no. of 1's at the I/P is odd no.

⇒ logical expression :-

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

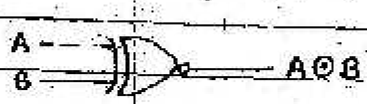
$$= 001 + 010 + 100 + 111 \rightarrow \text{odd no. of 1's.}$$

$$Y = \Sigma m(1,2,4,7)$$

⇒ The reduced form of this expression is,

$A\oplus B\oplus C$

EXNOR or XNOR :-



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

⇒ Whenever the I/p is same O/p is High.

SOP expression = $\bar{A}\bar{B} + AB$

POS expression = $(A+\bar{B})(\bar{A}+B)$

EXOR :-	$\bar{A}B + A\bar{B}$ ← SOP →	EXNOR :- $\bar{A}\bar{B} + AB$
	$(A+B)(\bar{A}+\bar{B})$ ← POS →	$(A+\bar{B})(\bar{A}+B)$

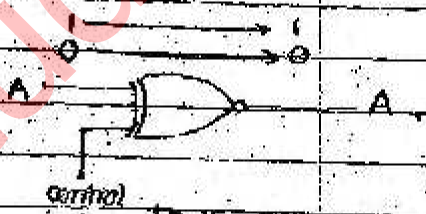
⇒ when A = B , then O/p is High.
therefore coincedence logic ckt and also called as equivalent detector.

⇒ When $A \neq B$, The O/p is low.

⇒ Enable and Disable :-

i) 

(inverter)

ii) 

(Buffer)

$A \odot A = 1$
$A \odot \bar{A} = 0$
$A \odot 0 = \bar{A}$
$A \odot 1 = A$

since, $A \odot A = 1$
$A \odot A \odot A = A$
$A \odot A \odot A \odot A = 1$
and so on.

$B \oplus B \oplus B \oplus \cdots\cdots\ n = 1$, if $n =$ even
B if $n =$ odd

⇒ EXOR and EXNOR is not always complement, it is complement only when the no. of I/p is even. and if I/p is odd then EXOR and EXNOR are same.

i.e. $A \oplus B \oplus C = A \odot B \odot C$ ⇒ same.

and, $A \oplus B \oplus C \oplus D = \overline{A \odot B \odot C \odot D}$ ⇒ complement

Ques:- Find expression of $A \odot B \odot C$.

Sol:- $A \odot B \odot C$

$= (\bar{A}\bar{B} + AB) \odot C$
$= (\overline{\bar{A}\bar{B} + AB})\bar{C} + (\bar{A}\bar{B} + AB)C$
$= (\overline{\bar{A}\bar{B}} \cdot \overline{AB})\bar{C} + (\bar{A}\bar{B} + AB)C$

Since, $\overline{(\bar{A}\bar{B} + AB)} = (\overline{A \odot B}) = A \oplus B = \bar{A}B + A\bar{B}$

$= (\bar{A}B + A\bar{B})\bar{C} + (\bar{A}\bar{B} + AB)C$
$= \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC$

$= A \oplus B \oplus C.$

Ques:- Minimize

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(A) $A \oplus B \oplus C$
(B) $A \odot B \odot C$
✓(C) $\overline{A \odot B \odot C}$
(D) $AB + BC + AC$

Sol:- for EXOR → O/P is 1 when odd no. of 1's at I/P.
In this case,

$$Y = \overline{A \oplus B \oplus C}$$

$$= \overline{A \odot B \odot C} \quad \text{Ans.}$$

⇒ EXOR and EXNOR are never always complemented, It is complement only when even variable occurs.

⇒ EXNOR gate is even no. of 1's detector when no. of I/P's are even.

⇒ EXNOR gate is odd no. of 1's detector when no. of I/P's are odd.

Problem:- $\bar{A} \oplus B = A \odot B$

Sol:- Put $X = \bar{A}$, $Y = B$

$X \oplus Y$

$= X\bar{Y} + \bar{X}Y$

$= \bar{A}\bar{B} + AB = A \odot B$.

Problem:- $\bar{\bar{A}} \oplus \bar{B}$

Sol:- Put $X = A$, $Y = \bar{B}$

$= X \oplus Y$

$= X\bar{Y} + Y\bar{X}$

$= AB + \bar{A}\bar{B}$

$= A \odot B$.

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Problem:- $A \oplus B \oplus AB$

Sol:- $(A\bar{B} + \bar{A}B) \oplus AB$

$= (A\bar{B} + \bar{A}B)\overline{AB} + \overline{(A\bar{B} + \bar{A}B)}\,AB$

$= A\bar{B}(\bar{A} + \bar{B}) + \bar{A}B(\bar{A} + \bar{B}) + (\overline{A\bar{B}} \cdot \overline{\bar{A}B})AB$

$= A\bar{B} + \bar{A}B + [(\bar{A} + B)(A + \bar{B})]AB$

$= A\bar{B} + \bar{A}B + [\bar{A}\bar{B} + AB]AB$

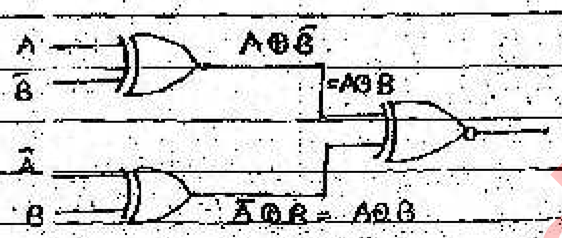
$= A\bar{B} + \bar{A}B + AB$

$= A(\bar{B} + B) + \bar{A}B = A + \bar{A}B$

$= (A + \bar{A})(A + B) = A + B$ Ans.

$$\boxed{A \oplus B \oplus AB = A + B}$$

Problem:-



Y = 1 ∵ $X \oplus X = 1$

$A \oplus 1$, Y = 1

(a) 0
(b) 1
(c) $A \oplus B$
(d) $A \odot B$

Sol:- Y = 1 Ans.

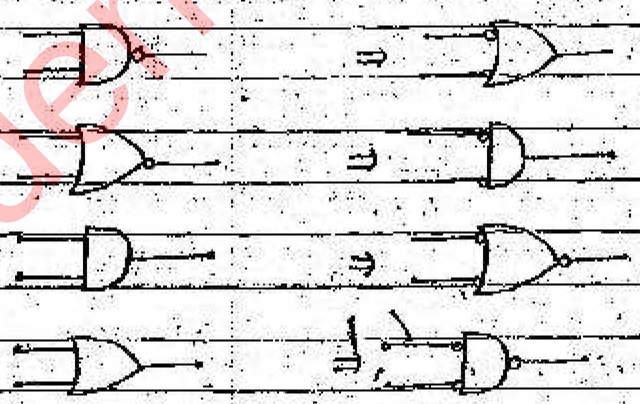
SYMBOLS :-

NAND ⇒ ⇒ Bubbled OR

NOR ⇒ ⇒ Bubbled AND

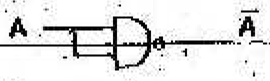
AND ⇒ ⇒

OR ⇒ ⇒



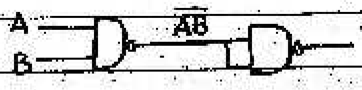
NAND as Universal :-

(i) NOT :-



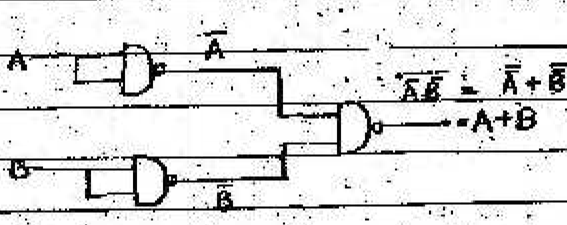
$\Rightarrow$ 1 gate required

(ii) AND :-



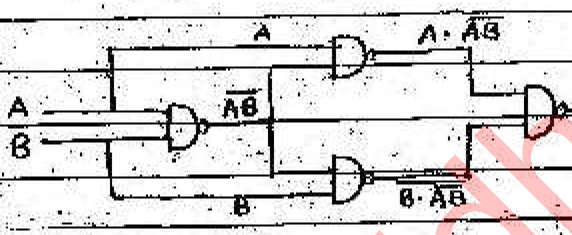
$\Rightarrow$ 2 gate

(iii) OR :-



$\overline{\bar{A}\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}}$ $\Rightarrow$ 3 gate.

(iv) EXOR :-



$Y = A \oplus B = \bar{A}B + A\bar{B}$

$\Rightarrow$ 4 Gate .

$$Y = \overline{\left(\overline{A \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}\right)}$$

$$= \left(A \cdot \overline{AB} + B \cdot \overline{AB}\right)$$

$$= \left(A(\bar{A}+\bar{B}) + B(\bar{A}+\bar{B})\right)$$

$$= A\bar{B} + B\bar{A} = A \oplus B$$

(v) EXNOR :-

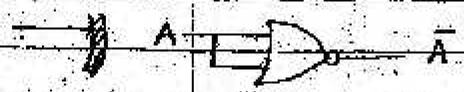
$\Rightarrow$ 5 Gate .

(vi) NOR :-

$\Rightarrow$ 4 Gate

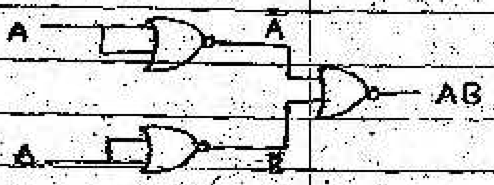
NOR As universal :-

(i) NOT :-



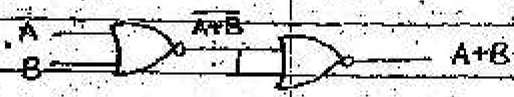
$\Rightarrow$ 1 gate

(ii) AND :-



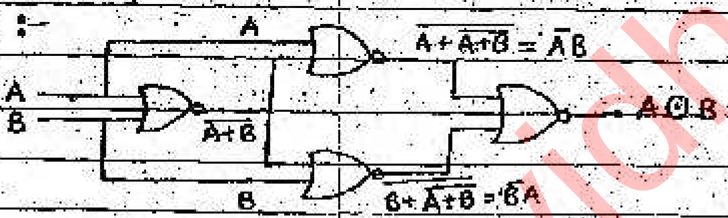
$\Rightarrow$ 3 gate

(iii) OR :-



$\Rightarrow$ 2 gate

(iv) EXNOR :-



$\Rightarrow$ 4 gate

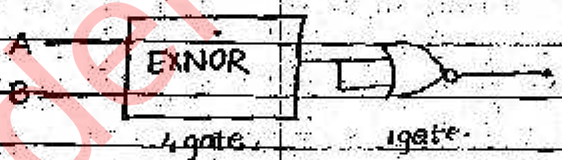
$y = \overline{(\overline{A+\overline{A+B}}) + (\overline{B+\overline{A+B}})} = \bar{A}(A+B) + \bar{B}(A+B)$

$= \bar{A}B + \bar{B}A = A\oplus B$

$\cancel{= (A+\overline{A+B})(B+\overline{A+B})}$

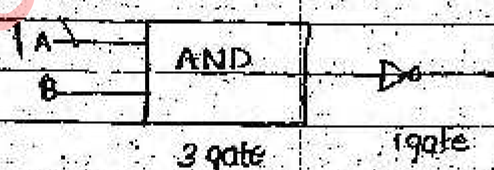
$\cancel{= AB + A(\bar{A}\bar{B}) + B(\bar{A}\bar{B}) + \bar{A}\bar{B}} = A\odot B$

(v) EXOR :-



$\Rightarrow$ 5 gate

(vi) NAND



$\Rightarrow$ 4 gate

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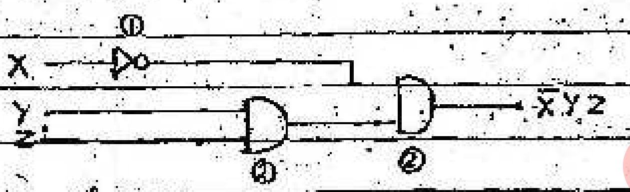
Note :-

logic gate	No. of NAND	No. of NOR
NOT	1	1
AND	2	3
OR	3	2
EXOR	4	5
EXNOR	5	4

Problem :- To implement $\bar{X}YZ$. The min no. of two I/P NAND gate required.

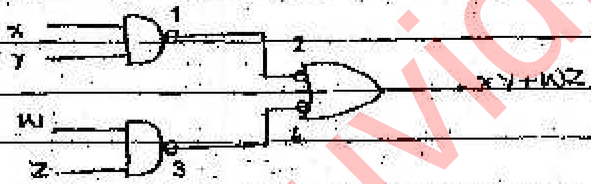
Sol :-



Total no. of NAND gate = 2+2+1 = 5 Ans.

Problem :- To implement XY + WZ, the min no. of 2 input NAND gate required.

Sol :-



⇒ 1^{st} inverter cancelled 2^{nd} and 3^{rd} cancelled 4^{th}

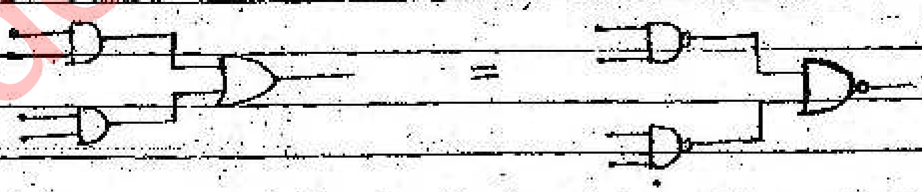
⇒ Now the total no. of NAND gate is.

= 2 + Bubbled OR (= NAND)

= 2 + 1 = 3.

= 3 NAND gate required

Note :-



Two level AND - OR = Two level NAND - NAND

$\boxed{\text{AND-OR = NAND-NAND}}$

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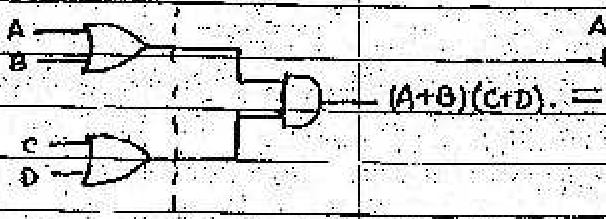
⇒ To implement SOP form, only NAND gate alone.

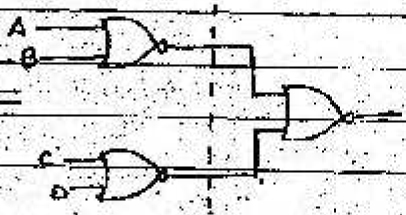
⇒ To implement POS form, only NOR gate alone.

Q:- if (A+B)(C+D) then min no. of Gate.

Sol^n:-



Two level OR - AND



Two level NOR - NOR.

⇒ $\boxed{\text{OR - AND} = \text{NOR - NOR}}$

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