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☆ ARITHMETIC OPERATION :-

(A) Binary Addition, subtraction, Multiplication :-

Q:- Add. 1 1 0 1 1 0
+ 1 0 1 1 0 1
1 1 0 0 0 1 1

Q:- Sub :- 1 0 1 1 0
0 0 1 0 1

Q. Multiply :

(a) 1 0 1 0
1 0 1 1

1 0 1 0
0 0 0 0
1 0 1 0
1 1 0 0 1 0

(b) 1 1 1 1
1 1 1 1

1 1 1 1
1 1 1 1
1 1 1 1 0
1 1 1 1 0 0
1 1 1 1 0 0 0
1 1 1 1 0 0 0 0
1 1 1 1 0 0 0 0 1

4 = 100
6 = 110
5 = 101

(B) Octal Addition, subtraction :-

0+0 = 0
0+1 = 1
1+1 = 2
1+7 = 10
7+2 = 11

7+1 = (8)$_{10}$ = 8 | 8 → 8 | 1 → 0 ↑ = (10)$_8$
0 1

7+7 = 8 | 14 → 8 | 1 → 6 ↑ = 16.
0 1

Sum of 2 octal no :-

(i) 2 4 3
+ 2 1 2
4 5 5

(ii) 5 6 7
+ 2 4 3
1 0 3 2

Q:- Subtract :- (base 8)

(i) 7 4 3
5 6 4
1 5 7

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(C) Hexadecimal (Add, Subtraction) :-

Addition :-

1+1 = 2
1+9 = A
A+A = $(20)_{10}$ = $(14)_{16}$
1+B = C

Q: (i) 5689 + 4574 = 9BFD

(ii) ADD + DAD = 1886A

Q: Subtract :

Sol (i) 974B − 587C = 3ECF

(ii) 9654 − 5321 = 4333

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(D) Complements :-

r = → (r-1)'s complement
→ r's complement

Binary → 1's, 2's
Octa → 7's, 8's
Decimal → 9's, 10's
Hexa → F's, 16's

(r-1)'s complement :-

⇒ Subtract from max. no. to the given no.

e.g. comp of (1010)

= 1111
1010
0101

To determine (r-1)'s compliment subtract given no from max. no. possible in the given base. (max. no. $(r^n - 1)$.)

e.g. 1's complement of 101101 is,

Sol:- 111111
− 101101
010010

Q:- determine 7's complement of octal no. 5674.

Sol:- 7777
− 5674
2103

Q:- Determine 9's compliment of decimal 2679.

Sol:- 9999
− 2679
7320

Q:- Det. F's comp. of Hexa. 2689.

Sol:- FFFF
2689
D976

...Associate

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(ii) r's complement :-

To determine r's complement first write (r-1)'s complement then add 1 at LSB. (at right most)

Q:- Det. 2's complement of 10100.

Sol.
```
  11111
- 10100
-------
  01011
+    1
-------
  01100  Ans.
```

Q:- Determine 2's complement of 10110.11.

Sol. 1's complement = 01001.00

+ 1

01001.01 Ans.

Q:- Determine 8's complement of octal 2670.

Sol. 7's comp :
```
  7777
- 2670
------
  5107
+    1
------
  5110
```

Q:- Determine 10's complement of Decimal 5690.

Sol. 9's =
```
  9999
- 5690
------
  4309
+    1
------
  4310
```

Q:- Determine 16's complement of Hexadecimal 5289.

Sol. ~~15's~~ F's =
```
  FFFF
- 5289
------
  AD76
+    1
------
  AD77
```

Problems

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CODES :-

1. BCD code :-

⇒ Binary coded decimal
⇒ weighted code.
⇒ 4 bit code.
⇒ 8421 code.
⇒ Each decimal digit with is represented with 4 bit

Decimal	BCD	Excess-3 code
0	0000	0011
1	0001	0100
2	0010	0101
3	0011	0110
4	0100	0111
5	0101	1000
6	0110	1001
7	0111	1010
8	1000	1011
9	1001	1100

1010, 1011, 1100, 1101, 1110, 1111 } invalid BCD code or don't care.

⇒ During Arithemetic operation if invalid BCD present then add 0110 to get correct result.

Problem:- A combinational ckt is applied with 4bit BCD code which is represented as $D_8 D_4 D_2 D_1$, o/p is Y., Y=1 then I/p BCD is divisible by 3. then logical expression for Y is.

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Sol. 0000 - 0
0011 - 3
0110 - 6
1001 - 9

$$Y = \bar{D}_8\bar{D}_4\bar{D}_2\bar{D}_1 + D_8\bar{D}_4\bar{D}_2\bar{D}_1 + D_8D_1 + D_8D_1 + D_2D_1\bar{D}_8 + D_2\bar{D}_1D_4$$

$$Y = \bar{D}_8\bar{D}_4\bar{D}_2\bar{D}_1 + D_1D_8 + D_1D_2\bar{D}_8 + \bar{D}_1D_2D_4$$

⇒ For write BCD code each digit (decimal) is write seperately in BCD.

e.g. $(534)_{10} = (0101\ 0011\ 0100)_{BCD}$

2. Excess -3 code :-

⇒ Excess -3 code = BCD +3

⇒ Unweighted code

⇒ 4 bit code.

Decimal	Excess -3 code.
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

Self complement.

⇒ It is self complement code.

⇒ Only unweighted code which is self complement is Excess 3-code.

⇒ The code which addition is 9 is self complement code.

e.g. 2421, 3321, 4311, 5211 } weighted } self complemented.

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Q1- Write 2421 weighted code.

Sol.

Decimal	2 4 2 1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	1 0 1 1
6	1 1 0 0
7	1 1 0 1
8	1 1 1 0
9	1 1 1 1

Self complement

rately

8. Binary to Gray code :-

(A) Binary to Gray :-

⇒ Unweighted code.

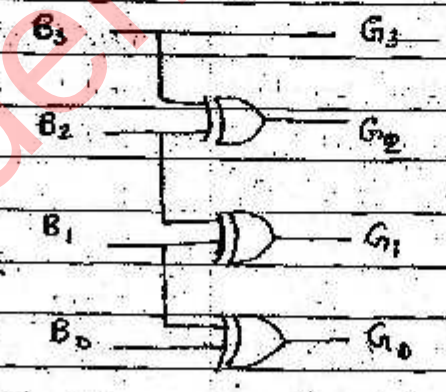
⇒ successive no. is differ by 1 bit.

⇒ Also called unit distance code.

⇒ Also cyclic code, Reflective code. and Minimum error code.

Binary 1 0 1 1 B_3 B_2 B_1 B_0

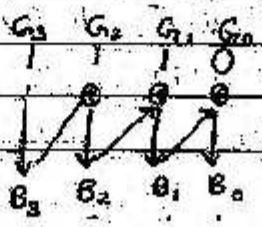
Gray. 1 1 1 0 G_3 G_2 G_1 G_0



excess

(B) Gray to Binary :-

Binary Gray



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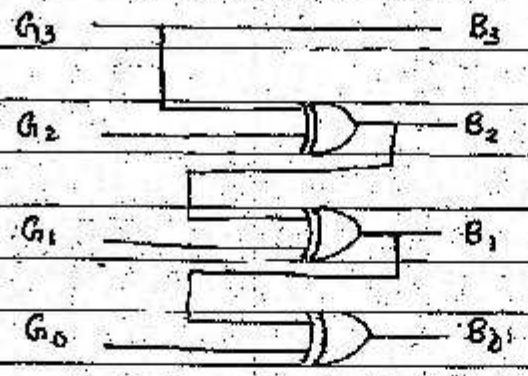

Q)
Sol

☆ Data Representation :-

Data representation

- Magnitude
  - unsigned
    - +ive
    - no sign bit
  - signed
    - +ive, -ive.
    - one extra bit → sign.
    - sign → MSB
    - logic - 0 → +ive
    - 1 → -ive.
- complement
  - 1's
    - +ive, -ive
  - 2's
    - +ive, -ive

Q:-1
Sol

	unsigned	signed	1's	2's
+6	110	0110	0110	0110
-6	X (can't write)	1110	1001	1010

⇒ In all representation +ive no. are represented in similar way. To represent -ive no in sign magnitude only sign bit change. In 1's complement represent -ive no., first write positive no. and then 1's complement to it.

⇒ And in 2's complement first write +ive no. and then 2's complement to it.

Q:⇒ A no. is represent in 2's complement for 1011 the equivalent decimal value.

Sol:- 1011 = -(0101) = -(0101)

= -5.

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Q:- To find 5-4 ?

Sol:- 5+(-4)

+5 = 0101 +5+(-4) = 0101

-4 = 1100 1100

* 0001

⇒ In 2's complement addition if any carry present it is discarded.

⇒ In 2's complement to extend no. of bit copy MSB bit

Q:-17. Page -(6):

Sol:- 1001 → -(0111) = -7

11001 → -(00111) = -7

111001 → -(000111) = -7

Binary	sign mag	1's	2's
0000	+0	+0	+0
0001	+1	+1	1
0010	+2	2	2
0011	+3	3	3
0100	+4	4	4
0101	+5	+5	+5
0110	+6	+6	+6
0111	+7	+7	+7
1000	-0	-7	-8 *
1001	-1	-6	-7
1010	-2	-5	-6
1011	-3	-4	-5
1100	-4	-3	-4
1101	-5	-2	-3
1110	-6	-1	-2
1111	-7	-0	-1

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4 bit :-

(i) range of signed mag. $-7 \rightarrow +7$

(ii) " " 1's complement $-7 \rightarrow +7$

(iii) " " 2's complement $-8 \rightarrow +7$

⇒ For signed mag. and 1's complement :-

n bit → $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

⇒ For 2's complement :-

n bit → $-(2^{n-1})$ to $+(2^{n-1}-1)$

Q:- Perform 5+4 using 2's complement.

Sol:-

$5 = 0101$

$4 = 0100$

1001 ✗

↳ overflow may occur when same (two) because sign no. are added in signed representation because for 4 bit we can only represent.

$-(2^{n-1})$ to $+(2^{n-1}-1)$ = $(-8 \rightarrow +7)$

let x and y are sign bit of two no. and z is resultant sign no. then condition for overflow is.

$z \rightarrow \boxed{\bar{x}\bar{y}z + xy\bar{z}}$ condition of overflow.

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let Cin = carry into MSB

Cout = carry from MSB

(two

ntation.

esultant

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Q: t

Sol

(i

=

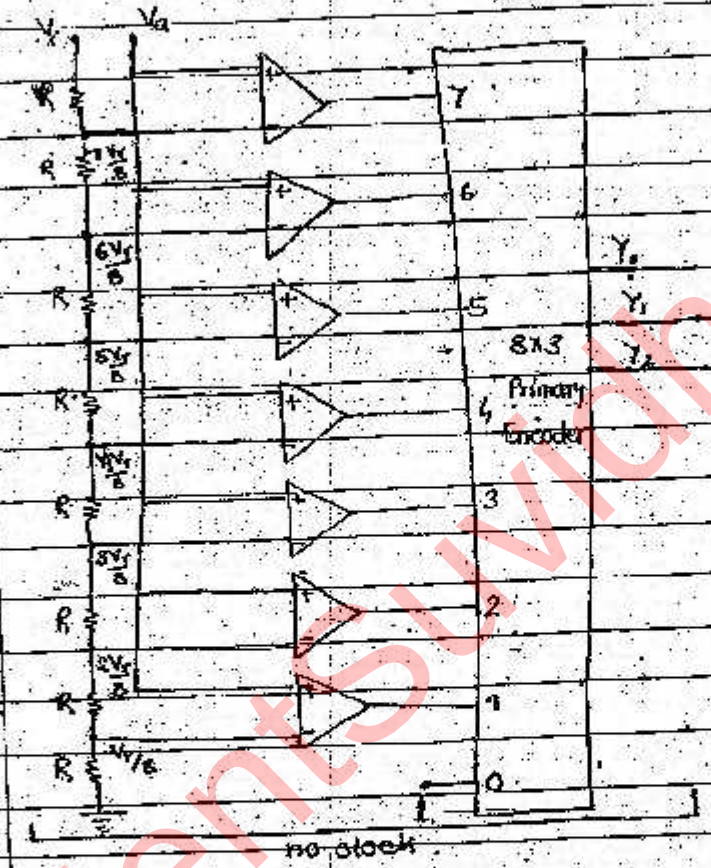
Q1- 10

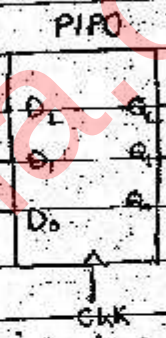
(B) Parallel comparator type :-

⇒ For n bit → $2^n - 1$ comparator required.
→ 2^n resistor required.
→ $2^n \times n$ priority encoder.

⇒ Also called Flash ADC (fastest ADC)

(B) 3 Bit parallel comparator :-



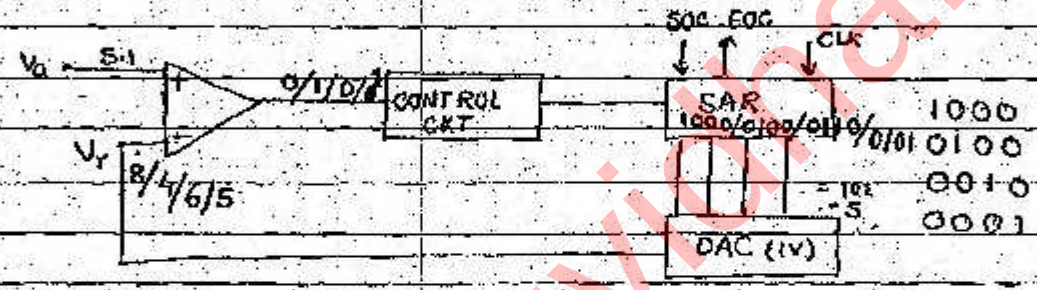


1 clock required.

⇒ No clock pulse is required.
⇒ Therefore it is fastest ADC among all.
⇒ Max no. of clock pulse required for n bit conversion is which is inside PIPO.

Range of analog	O/P
$V_a > 7V_r/8$	1 1 1
$7V_r/8 > V_a > 6V_r/8$	1 1 0
$6V_r/8 > V_a > 5V_r/8$	1 0 1
$5V_r/8 > V_a > 4V_r/8$	1 0 0
$4V_r/8 > V_a > 3V_r/8$	0 1 1
$3V_r/8 > V_a > 2V_r/8$	0 1 0
$2V_r/8 > V_a > V_r/8$	0 0 1
$V_r/8 > V_a$	0 0 0

(c) SAR Type (Successive approximation Register) :-



SOC - Start of conversion
EOC - End of conversion

⇒ Ring counter is used to set the base.
⇒ Control ckt is used to reset ($V_a < V_r$)

⇒ In SAR Type ADC, ring counter will present to successively set the base.
⇒ control ckt is used to reset, previously set bit when $V_a < V_r$.
⇒ In SAR Type ADC, n clock pulse required for n bit conversion.
⇒ conversion time = nT_{CLK}

⇒ SAR Type, conversion time uniform for any analog voltage. (conversion time is independent of

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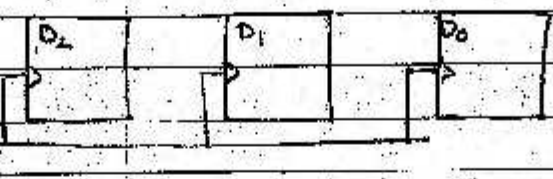
Q: Design a synchronous counter using D-FF for the sequence.
0→2→5→3→6→4→7→0.

Sol: (i)



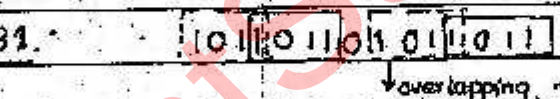
since 1,6 is unused
used lock out condition
i.e. 1 → 0
6 → 0

(ii) Truth table:-

PS	NS
$Q_2\ Q_1\ Q_0$	$Q_{2+}\ Q_{1+}\ Q_{0+}$
0 0 0	0 1 0
0 1 0	1 0 1
1 0 1	0 1 1
0 1 1	1 0 0
1 0 0	1 1 1
1 1 1	0 0 0
0 0 1	0 0 0
1 1 0	0 0 0

⇒ To avoid lock out change unused states into one of used states in state table.

Q: 10 or, 31.



⇒ 4bit ⇒ 4 state requires ⇒ 2 FF. required.

Moore & Mealy :-

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State Machines

Moore

⇒ O/P depend on present state

⇒ Design easy

⇒ More no. of state

Mealy

⇒ O/P depend on Present st
Present I/

⇒ Design complex

⇒ less no. of state.

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(a) counter type ADC
(b) SAR type ADC
(c) Parallel comparator type
(d) dual slope integrating type.

(i) Weighted resistor
(ii) R-2R ladder.

(A) Digital to Analog converter (DAC) :-

(1) Resolution / step size.
(2) Analog o/p voltage.
(3) V_{FS}
(4) % Resolution (5) Error Accuracy.

1. Resolution / Step size :-

It change in analog voltage corresponding one lsb increment in the I/p.

$$\text{Resolution} = \frac{V_r}{2^n - 1}$$

where V_r = reference voltage corresponding to logic 1
n = no. of bits.

2. Analog o/p voltage :-

V_{analog} = Resolution × Decimal equivalent of binary data

Q. In a 4 bit DAC reference voltage 5V. if binary data 1001 is applied then analog voltage is.

Sol:

$$\text{Resolution} = \frac{V_r}{2^n - 1} = \frac{5}{16-1} = \frac{1}{3}$$

$$V_{analog} = \frac{1}{3} \times 9 = 3V.$$

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(3) V_{FS} :-

Full scale voltage is the max. o/p voltage of DAC.

$$V_{FS} = \frac{V_r}{2^n - 1} \times 2^n - 1$$

$$\boxed{V_{FS} = V_r}$$

(4) % Resolution :-

$$\boxed{\% \text{ Resolution} = \frac{\text{Resolution}}{V_{FS}} \times 100}$$

$$\boxed{\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100}$$

(5) Errors / Accuracy :-

⇒ Max. error acceptable in ADC's or DAC's is equal to resolution or step size.

(B) Analog to Digital converter :-

Characteristics of ADC's :-

(1) $$\boxed{\text{Resolution} = \frac{V_{range}}{2^n - 1}}$$

where,

$V_{range} = V_{max} - V_{min}$.

(2) $$\boxed{\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100}$$

(3) $$\boxed{\text{Dynamic range} = (6n + 1.76)\ dB \approx 6n\ dB}$$

Ques :-

Sol° -

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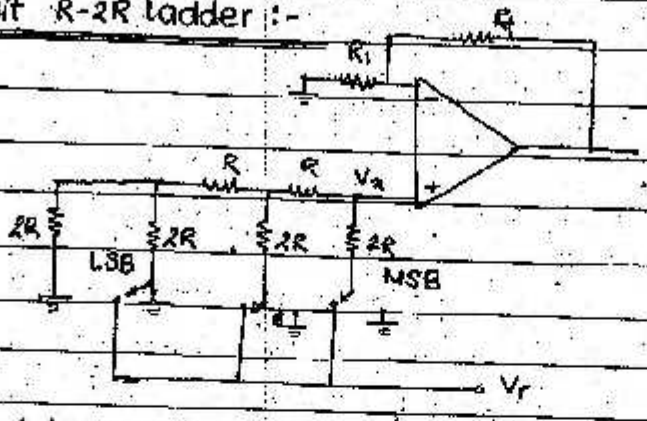
(B) R-2R ladder :-

→ Normal ladder
→ Inverted ladder

* Non inverting
* Inverting.

(B1) 3 Bit R-2R ladder :-



⇒ Adjecent to 2R is LSB.

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_a$$

V_a = Resolution * Decimal equivalent of Binary data.

$$= \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i$$

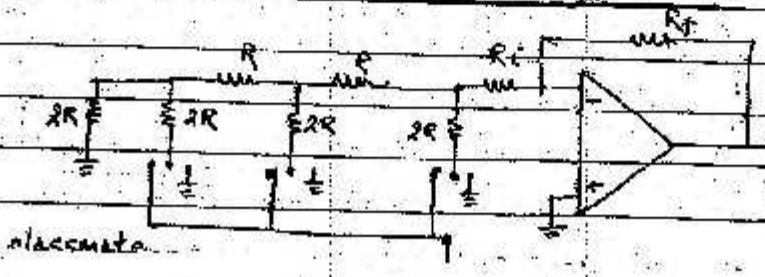
(decimal equivalent = $b_2 b_1 b_0$ (binary data))

$$= b_2 2^2 + b_1 2^1 + b_0 2^0 = \sum_{i=0}^{n-1} 2^i b_i$$

$$\boxed{V_o = \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i * \left(1 + \frac{R_f}{R_1}\right)}$$

V_o = Resolution * Decimal * gain.

(B2) 3 Bit R-2R ladder (Inverting) :-



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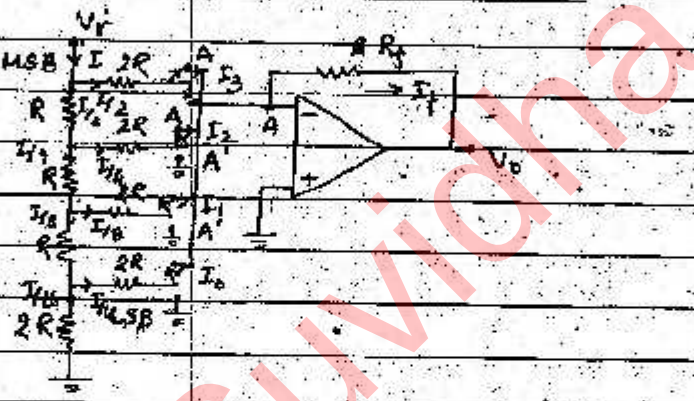
V_o = Resolution * decimal * gain.

$$V_o = \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i * \left[\frac{-R_f}{R_1+R}\right]$$

$$I_f = \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i * \left[\frac{+1}{R_1+R}\right]$$

(β_3) Inverted ladder type DAC circuit :-



⇒ Since A and A' both are ground then (logical or virtual ground and ground) the switch is at same potential then charging and discharging of switch problem removed in previous ckt.

$$I = V_r/R$$

$$I_3 = \frac{I}{2} \times b_3$$

$$I_2 = \frac{I}{4} \times b_2$$

$$I_1 = \frac{I}{8} \times b_1$$

$$I_0 = \frac{I}{16} \times b_0$$

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Resolution of R-2R ladder type DAC's is :-

$$\text{Resolution} = \frac{V_r}{2^n}$$

Ques- 5. Page 41.

Sol^n -

$V_{FS} = 10.24$

$n = 10$

$$\text{Resolution} = \frac{10.24}{2^{10}} = 10\text{mV}.$$

$$\text{error} = \frac{LSB}{2} = \frac{10\text{mV}}{2} = \pm 5\text{mV}$$

calibarate at 25° i.e. error at 25°c is zero.

$\Rightarrow \pm 25°c \Rightarrow 5\text{mV}$

$$1°c = \frac{5}{25°c}\text{mV}$$

$$= 0.2\ \text{mV/°c} = 200\mu\text{V/°c}.$$

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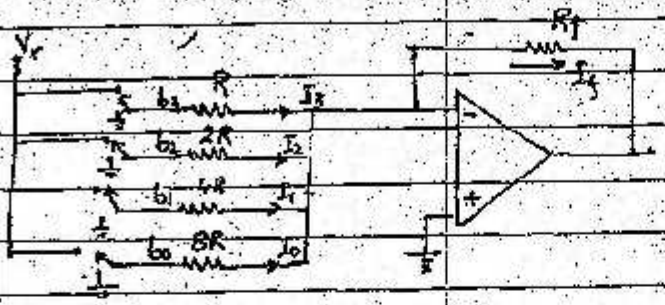
(A) Digital to Analog Circuit :- (B)

Digital to Analog circuits :-

(A) Weighted Resistor DAC :- (4 Bit) :-



(B1)

b_3 = MSB = more current

b_0 = LSB = less current

$$I_3 = \frac{V_r}{R} * b_3$$

$$I_2 = \frac{V_r}{2R} * b_2$$

$$I_1 = \frac{V_r}{4R} * b_1$$

$$I_0 = \frac{V_r}{8R} * b_0$$

$$I_f = I_3 + I_2 + I_1 + I_0$$

$$V_0 = -I_f R_f$$

LSB resistance = (2^{n-1}) MSB resistance.

⇒ In weighted resistor DAC the accuracy is less due to use of different resistance.

⇒ To overcome this we use R-2R ladder used. (B2)

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$$I_f = I_0 + I + I_2 + I_3$$

$$= \frac{I}{16}\left[8b_3 + 4b_2 + 2b_1 + b_0\right]$$

$$= \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right) \times \frac{1}{R}$$

$$\boxed{I_f = \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right)\frac{1}{R}}$$

$$\boxed{V_0 = \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right)\left(\frac{-R_f}{R}\right)}$$

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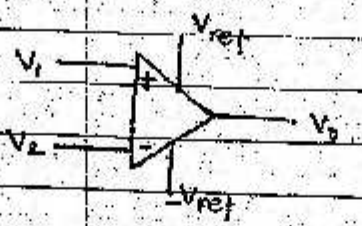
Analog to Digital circuit :-

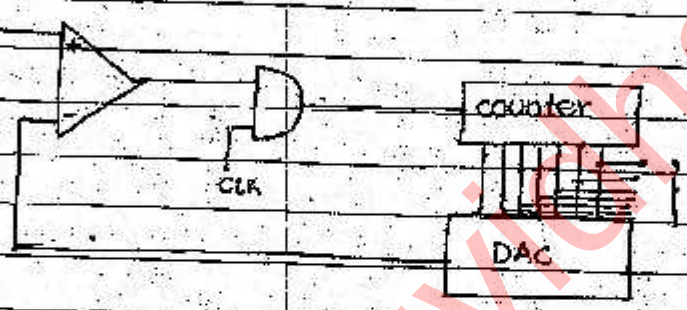
(A) Counter type ADC :-



$V_1 > V_2 \Rightarrow V_0 = V_{ref}$

$V_1 < V_2 \Rightarrow V_0 = -V_{ref}$

⇒ It is one bit quantizer.



⇒ In counter type ADC a comparator is used in I/P stage to compare I/P analog voltage with reference volta provided by DAC feedback.

⇒ A counter is used to count no. of clock pulses appli

⇒ when analog voltage (V_a) is greater than DAC voltage then o/p is 1. then counter count and if analog voltage (V_a) is less than reference voltage (DAC voltage) then o/p is 0 and counter stops counting and it give the comparative digital o/p.

⇒ Max. no. of clock pulses required for N bit conversion is $2^n - 1$.

⇒ Max. conversion time $= (2^n - 1)\, T_{CLK}$.

⇒ Conversion time depends on I/P analog voltage.

⇒ Also called Ramp type ADC.

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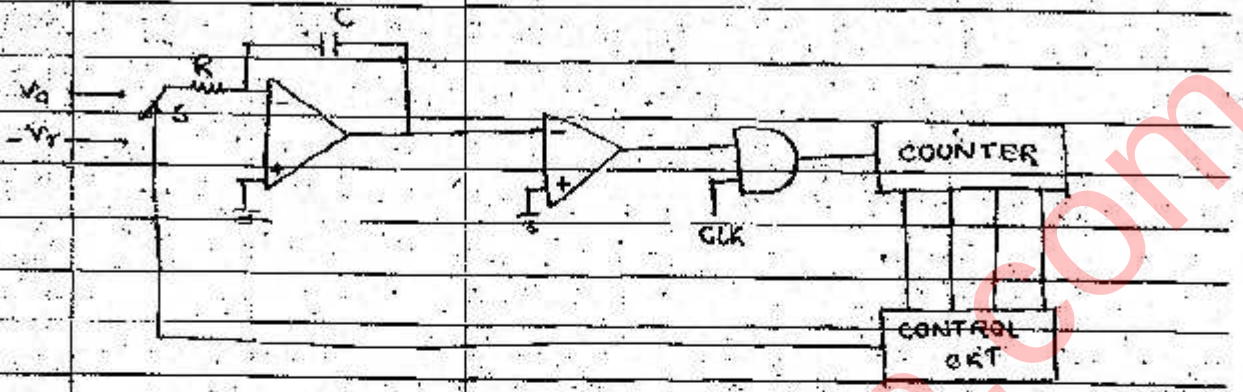
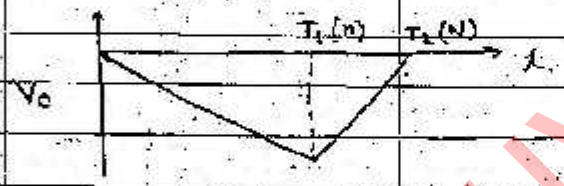
⇒ SAR is mostly used in Digital ckt to provide interface with microprocessor.

(D) Dual slope Integrating type ADC :-



⇒ V_r slope is always greater than V_a slope.



$$T_1 = 2^n T_{CLK}$$
$$T_2 = N T_{CLK}$$

⇒ In Dual slope a counter is used to count clock pulse
⇒ conveption started initially counter is reset to zero and switch s is connected to V_a (analog voltage) with integrater is integrating analog voltage o/p of integrate will becom -ive voltage. due to this comparator o/p 1 and counter continues cntd clock pulses, after 2^n CLK pulses again counter value became zero. at this time t_1 control ckt connect switch S to $-V_e$. During V_R integration upto T_2 time o/p of integrator is -ive. due to this counter again contin clock pulses. at time T_2 o/p of integrator become -ve and comparator o/p became 0 due to this counte

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will stops. let N is count when counter stops.

Then,

$$V_o = -\frac{V_a}{RC} \cdot T_1 + \frac{V_r}{RC} (T_2 - T_1)$$

at time $t = T_2$, $V_o = 0$

$$\Rightarrow 0 = -\frac{V_a}{RC} \cdot T_1 + \frac{V_r}{RC} (T_2 - T_1)$$

$$\Rightarrow V_a T_1 = V_r (T_2 - T_1)$$

$$\Rightarrow V_a \cdot 2^n T_{CLK} = V_r \cdot (N T_{CLK})$$

$$\Rightarrow N = \frac{V_a \cdot 2^n}{V_r} = \frac{V_a 2^n}{V_r}$$

$$\Rightarrow V_a = \frac{V_r}{2^n} N$$

$$\boxed{V_a = \frac{V_r}{2^n} \cdot N}$$

If $V_r = 2^n$ then,

$$\boxed{V_a = N}$$

⇒ This is the most accurate ADC among all.

⇒ All ripple and noise is seperated or compressed by capacitor. (Therefore this have more accuracy due to integrator).

⇒ max. no. of clock pulse $= 2^n + 2^n - 1$

$\approx 2^n + 2^n = 2^{n+1}$.

⇒ It is slowest among all.

Application :-

⇒ Mostly used in digital voltmeter.

Clock pulse :-

(i) Counter type $= 2^n - 1$ (ii) Flash $= 1$

(iii) SAR $= n$ (iv) Dual type $= 2^{n+1}$

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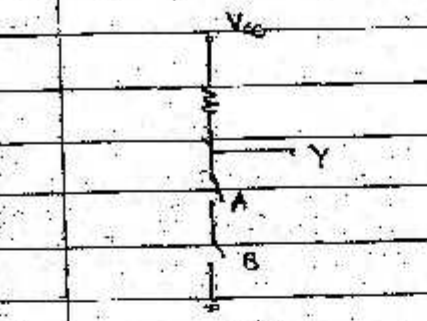
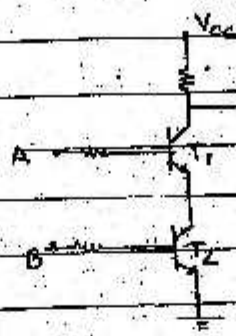
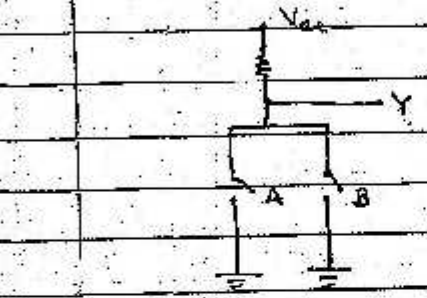
4. NAND Gate :-

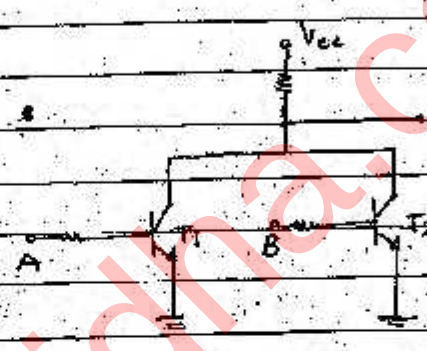




A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR Gate :-

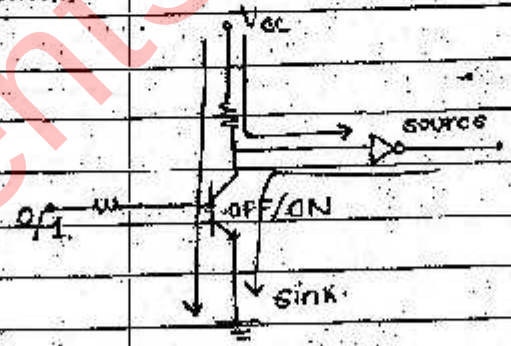




A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

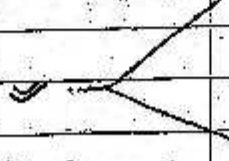
⇒ When logic gate o/p is 1. (Tr. OFF) it will act as current source.

⇒ When logic gate o/p is 0 (Tr. ON) it will act as current sink.



⇒ In cutoff and saturation region transistor will act as switch.

J_E	J_C	Region
RB	RB	cutoff
RB	FB	Reverse active
FB	RB	Active
FB	FB	SATURATION



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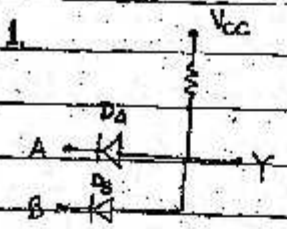
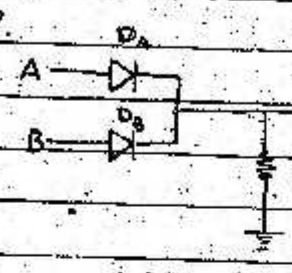
1. 

(Diode AND Gate)

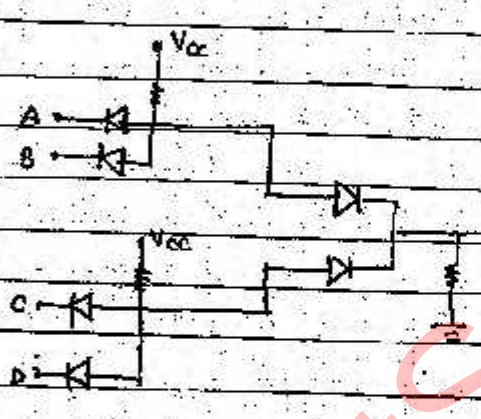
A	B	D_A	D_B	Y
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1

2. 

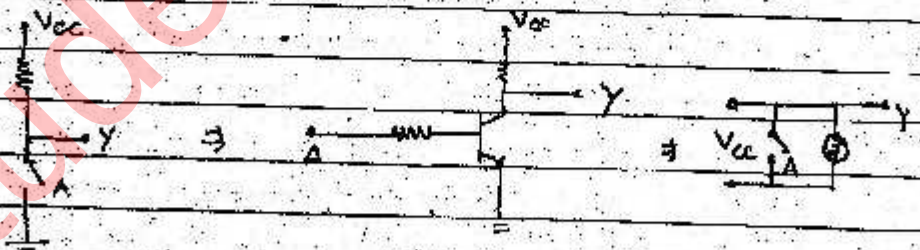
$V_0 = A + B$

(Diod OR Gate)

⇒ For Not gate we use transistor.

Problem:- 

Sol":- $V_0 = AB + CD$

3. NOT :- 

if A = 0, Tr is cutoff, Y = 1.

if A = 1, Tr is sat, Y = 0

discrete

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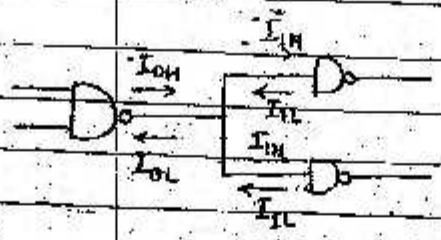
iv) Fan out :-

It is max. no. of logic gate that can be given by a logic gate.



$$fanout_H = \frac{I_{OH}}{I_{IH}}$$

$$fanout_L = \frac{I_{OL}}{I_{IL}}$$

⇒ Max. fan out is min value of $(fanout_H, fanout_L)$.

Ques:- If $I_{OH} = 400\mu A$, $I_{IH} = 40\mu A$, $I_{OL} = -16mA$, $I_{IL} = 1.6m$ find fanout.

Sol:- $fanout_H = \frac{400}{40} = 10$

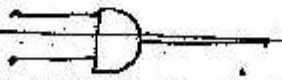
$fanout_L = \frac{16}{1.6} = 10.$

max. fan out $= (10, 10)_{min} = 10.$

⇒ TTL have max. fanout.

v) Noise Margin :-

It is the max. noise voltage that can be added to the logic family which will not affect the o/p.



$V_{IL} \leftarrow 0$ $\quad 0 \rightarrow V_{OL}$

$V_{IH} \leftarrow 1$ $\quad 1 \rightarrow V_{OH}$

$$V_{OH} > V_{IH} > V_{IL} > V_{OL}$$

High level NM_H $\quad$ Low level NM_L

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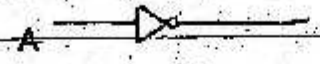
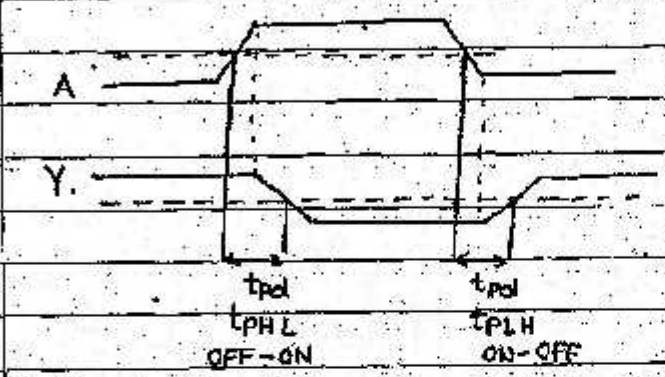
Characteristics of logic family :-

(i) Propogation delay :- (t_{Pd}) :-

⇒ It is measured in nsec.





$$t_{pd} = \frac{t_{PHL} + t_{PLH}}{2}$$

⇒ Propogation delay is always measured from 50% value of the diag.

⇒ In Tr, ON to OFF time is more compare to OFF to ON time due to saturation or storatge time.

(ii) Power dissipation :-

⇒ Power dissipation by each logic gate.

⇒ P_{diss} = mw.

$$P_{diss} = V_{cc} \cdot I_{cavg}$$

(iii) Figure of Merit :-

$$FOM = P_{diss} * t_{pd} \quad = \text{PJoule.}$$

⇒ I^2L have best FOM.

⇒ Value of FOM is low the logic family is best

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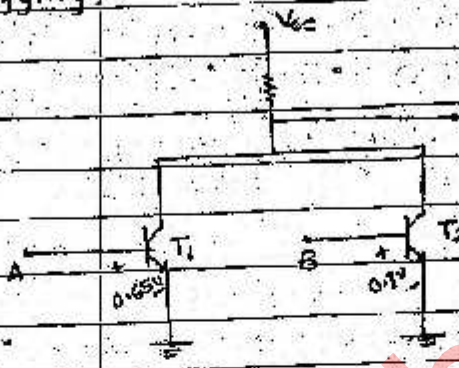
(B) DCTL (Direct Coupled Transistor logic) :-

⇒ In RTL logic family if i/p resistance removed then resultant is DCTL.

⇒ & t_{pd} = 40 nsec.

Disadvantage :-

⇒ current Hogging



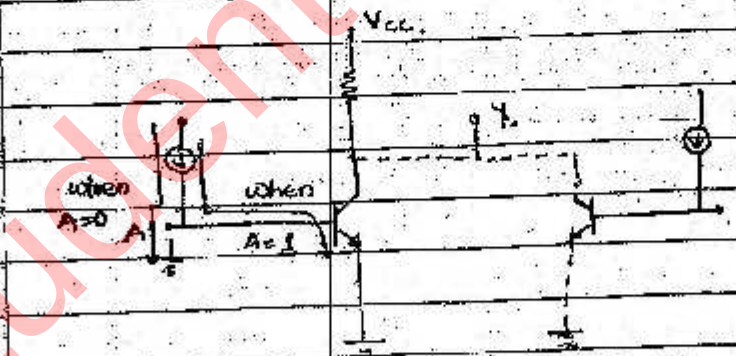
A	B	T_1	T_2	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	0

due to current Hogging

⇒ In DCTL logic, if Tr. switch different characteristics are used the Tr having lower $V_{BE(SAT)}$ then first ON and it will not allow other Tr to ON. this phenomenon is known as current Hogging.

Integrated Injection logic (I^2L) :-

⇒ It's injecting the current into Base.



⇒ When A is high the current flows through the base of Tr.

⇒ i.e. T_1 must be ON.

⇒ I^2L covers less space.

⇒ ie I^2L have high density.

⇒ It is equivalent to NOT gate.

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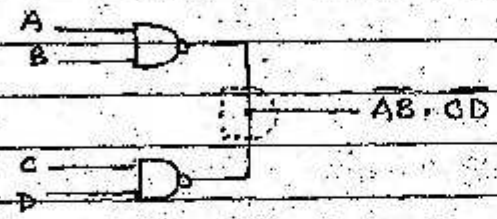
$NM_H = V_{OH} - V_{IH}$

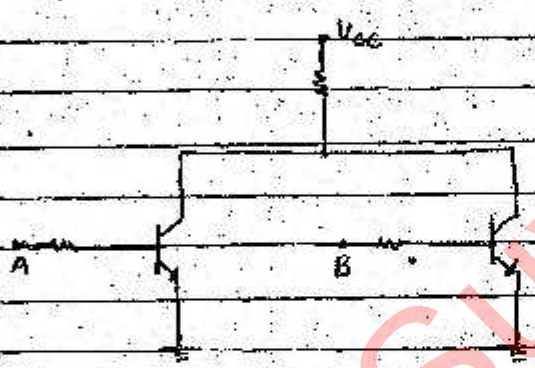
$NM_L = V_{IL} - V_{OL}$

overall noise margin = $(NM_H, NM_L)_{min}$

(A) RTL (Register Transistor logic) family :-



(wired AND)



⇒ Basic gate - NOR gate.

⇒ t_{pd} = 50ns

⇒ P_{diss} = 10 mW

⇒ FOM = 500 PJ

⇒ NM = 0.2 V

⇒ Fanout = 3

⇒ Wired AND used.

Disadvantage :-

1. lower speed of operation.
2. low Noise margin
3. lowest fan out

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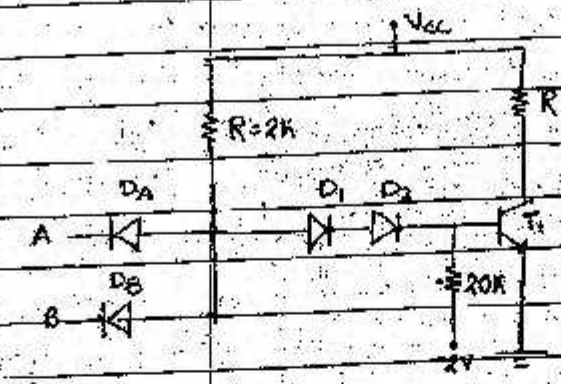
DTL (Diode Transistor logic) family :-

⇒ AND Gate followed by NOT gate.



A	B	T_1	Y
0	0	OFF	1
0	1	OFF	1
1	0	OFF	1
1	1	ON	0

⇒ 20K resister used only for discharging the junction capacitance. The capacitance which is discharge is Transitron cap. C_c.

⇒ The ckt is called basic DTL gate.

⇒ In this any one of the I/P is low. or all the I/P are low, D_A and or D_B will become forward bias where as D_1 and D_2 will become reverse bias. due to this Tr T_1 is OFF and o/p is 1.

⇒ When all the I/P's are high then D_A and D_B become reverse bias and D_1 and D_2 will become forward bias and T_1 is ON and o/p is low.

more

⇒ The basic gate is NAND gate.

⇒ t_{pd} = 30ns.

⇒ P_{diss} = 8 mw.

⇒ PDM = 240 PJ

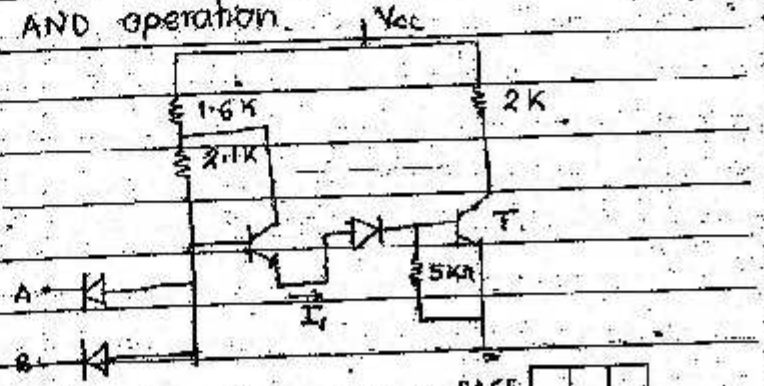
⇒ NM = 0.75 V.

⇒ Fanout = 3.

⇒ It provides wired AND operation.

⇒ To increase fanout we introduce Tr in place of Diode.

⇒ 5 KΩ resistor used to lower the I_1 current.



called STANDARD LOGIC

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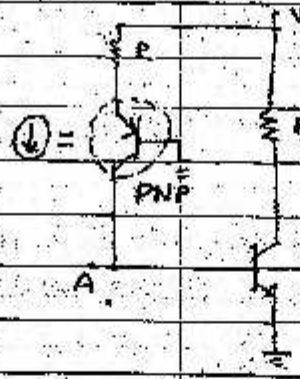

⇒ There is no problem of current Hogging.

⇒ PDM = 0.1 PJ – 0.7 PJ.
Best PDM among all logic family.

⇒ t_{pd} = 40ns.

⇒ Fan out = 8.

SSI	–	1-12
MSI	–	13-99
LSI	–	100-1000
VLSI	–	>1000.

no of gates used in this integration.

⇒ In I^2L logic, due to integration of PNP and NPN tr. it occupies less area hence density are more in I^2L logic. It is mostly used in MSI and LSI logic family.

⇒ Also called MTL (Merged logic family) due to integration of Transistor.

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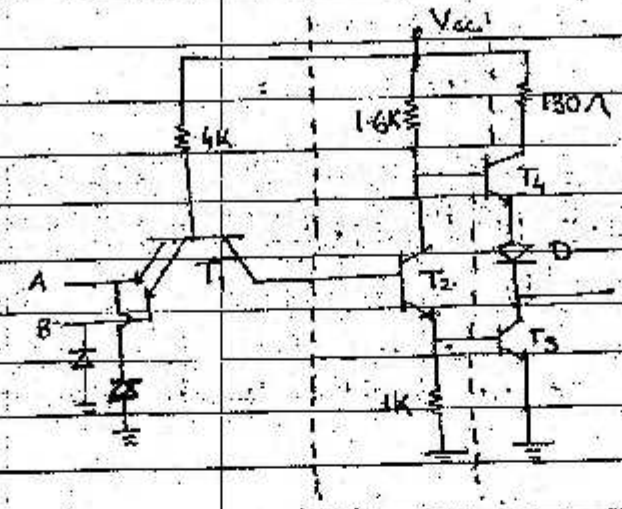
TTL (Transistor Transistor logic) family :-



T_1 = Multiemitter transistor.

A	B	T_1	T_2	T_3	T_4	Y
0	0	A	C	C	S	1
0	1	A	C	C	S	1
1	0	A	C	C	S	1
1	1	R	S	S	C	0

⇒ The ckt shown in fig. is standard TTL logic family. it basically have three stage.

(i) Multiemitter I/p stage
(ii) Phase splitter
(iii) Totem pole or, active pull up o/p stage.
active = use of Tr T_4
Pull up = Tr (T_4) connect to V_{cc}.

Operation :-

⇒ Any one of I/p low or all I/p's are low then EB junction is FB. (J_E = FB) and collector base (J_C = RB) is RB. Tr. is in active mode. due to this Tr. T_2 and T_3 are OFF (in cutoff region) where as T_4 in is SAT Hence o/p is 1.

⇒ When all the I/p's are high then J_E (EB Junct°) of T_1 is RB. and J_C (CB Junct°) is FB. (The mode of operation is Reverse active.

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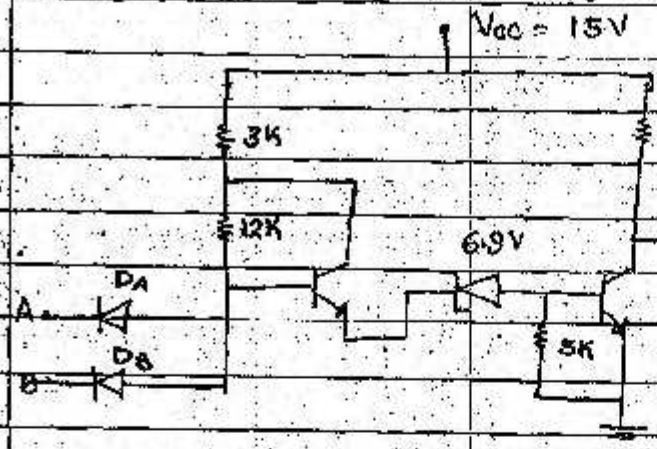
High Threshold logic (HTL) family :-



- ⇒ Zener Diode is used in place of D_2
- ⇒ NM = 4 - 5V (Highest noise margin)
- ⇒ since in DTL all diode and Transistor is -ive temp coefficient ($\frac{dV}{dT}$ = e - 2.5 mv/°c
- ⇒ logic 0 = 2V, logic 1 = 12V } Higher voltage swing
- ⇒ t_{pd} = 90 ns
- ⇒ P_{diss} = 55 mw
- ⇒ PDM = 4950 PJ ≈ 5000 PJ
- ⇒ Fanout = 8
- ⇒ Basic gate = NAND gate
- ⇒ Noise margin = 4V - 5V

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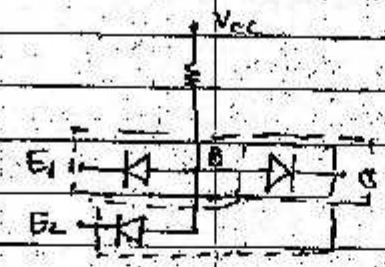
T_2 and T_3 are in saturation and T_4 is in cutoff. Hence o/p is zero.



$V_{IH} = 2\ V$ → I/p voltage at which T_r takes logic

$V_{OH} = 2.4\ V$

$V_{IL} = 0.8$

$V_{IH} = 0.4$

$t_{pd} = 10\ ns$

$P_{diss} = 10\ mw$

FOM = 100 PJ

Fanout = 10

NM = 0.4V.

⇒ Diode D is used to cutoff Tr T_4 when T_3 is ON.

⇒ Advantage of Totem pole :-

1. lower power dissipation.
2. Higher speed of operation.
3. Higher fan out

⇒ Disadvantage of Totem pole :-

It is not used in wired logic.

⇒ To provide wired AND logic open collector configuration is used.

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⇒ 130 Ω resistor used in collector in o/p stage to reduce ripple or noise generation. to in the high frequency of operation.

⇒ In TTL if any I/p is open it behaves as logic 1.

⇒ Clamping diodes are connected in I/p stage to protec transistor during high frequency of operation.

→ ringing.

⇒ clamping D, removes ringing of high frequency operation.

⇒ There are different type of TTL:-

(a) standard TTL
(b) High speed
(c) low power
(d) Schottky TTL.

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High speed TTL :-

In standard TTL logic family if Resistor value reduce then t_{pd} reduces and known as High speed logic family.

t_{pd} = 6nsec.

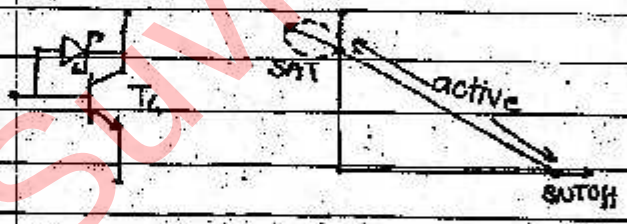
⇒ Power dissipation increases.

Low speed power TTL :-

In TTL logic family if Resistor value increased then power dissipation reduced and resultant is known as low power logic family.

Schottky diode :-

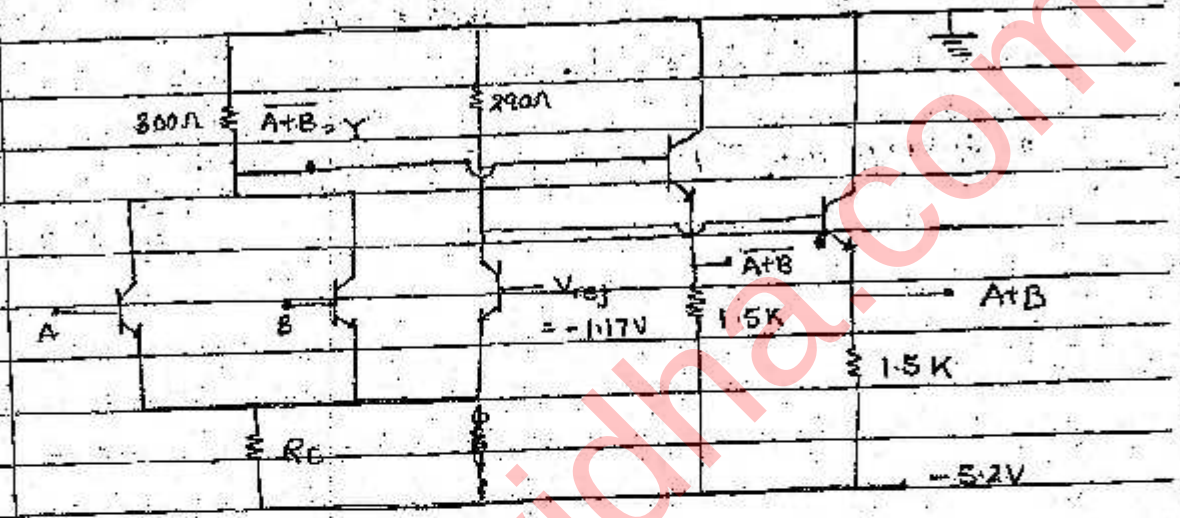
If schottky diode is used b/w collector and Base region then it will remove storage time and saturation delay. the family known as schottky diode TTL.



t_{pd} = 2nsec.

ECL (Emitter coupled logic family) :-

⇒ It is never go in saturation region.
⇒ work only in cutoff and Active region.
⇒ It is fastest logic family due to work in a Active and cutoff region. (Because it is non saturated)



t_{pd} = 1nsec
fanout = 25

⇒ It basically contains contains two stage.
(1) Differential amp^r I/p stage.
(2) CC or Emitter follower o/p stage.
⇒ Due to use of D.A. complementry o/p are available in ECL logic family. (NOR/OR) gate.
⇒ Due to use of CC stage in the o/p fanout is high.
⇒ Negative spikes do not affect the transistor, due to -ive power supply.
⇒ ECL uses -ive power supply. Due to this any spikes or negative voltage not affect operation.

t_{pd} = 1ns
P_{diss} = 55 mw
PDM = 55 PJ
Fanout = 25
N.M = 0.3V

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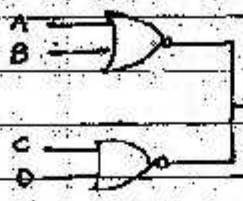
logic 0 = -1.7V
logic 1 = -0.85V.

} It is logic L mode only voltage supply is negative

⇒ ECL provide wired AND logic



$(A+B)+(C+D)$

⇒ If any I/p is open then it is logic '0'.

⇒

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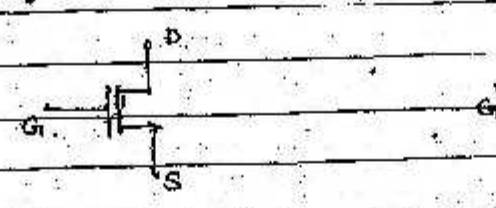
NMOS :-



N-channel :-

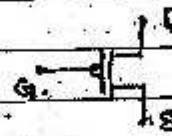
logic '0' = OFF

logic 1 = ON.

P- channel MOS :-

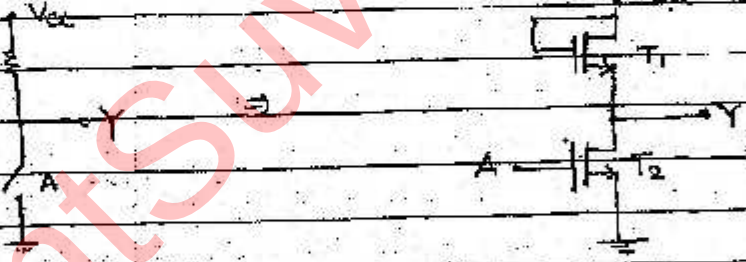
logic '0' = ON

logic 1 = OFF



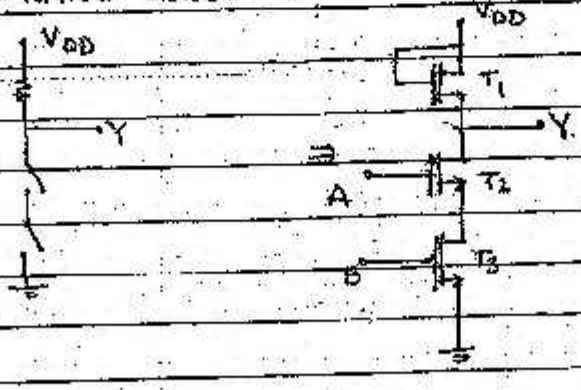
⇒ Since FET is voltage variable resistor hence in MOS circuit in place of req. resistor we use MOSFET.

NMOS NOT Gate :-



A	T_2	Y
0	OFF	1
1	ON	0

NMOS NAND Gate :-



A	B	T_2	T_3	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

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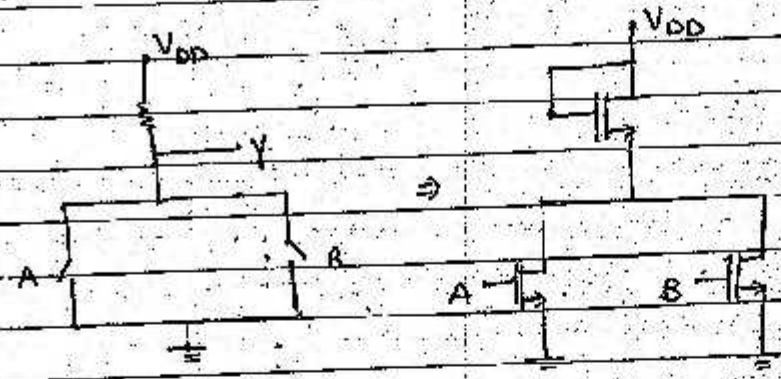
NMOS NOR Gate :-



t_{pd} = 250 nsec

P_{diss} = 1mW

PDM = 250 PJ

fanout = 5

NM = 1·5 V

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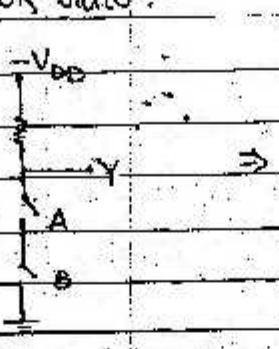
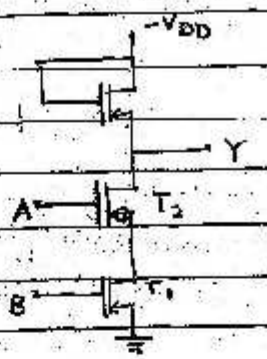
PMOS NOR Gate :-



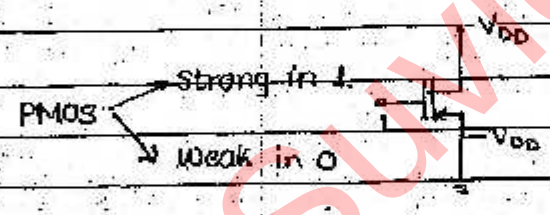


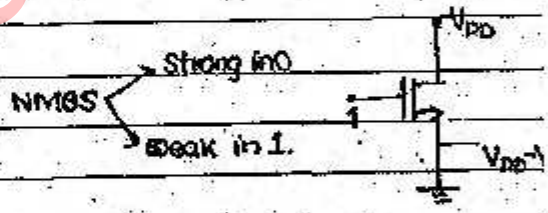
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

t_{pd} = 300 nsec

P_{diss} = 0.2 mW

FOM = 60 PJ.





Where, V_T = Threshold voltage.

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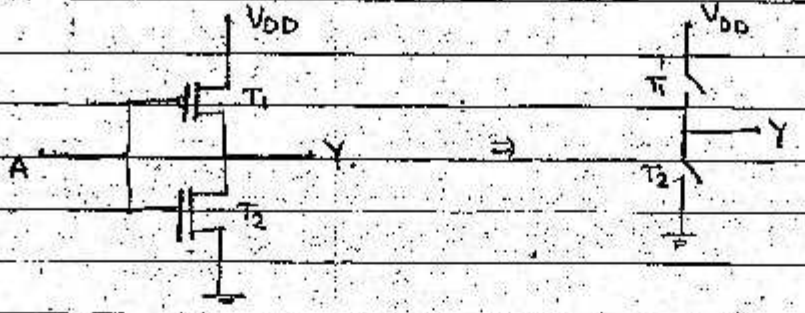
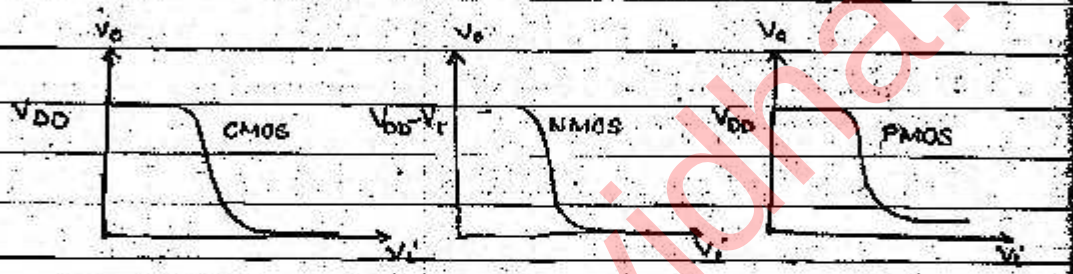
CMOS NOT Gate :-



A	T_1	T_2	Y
0	ON	OFF	1
1	OFF	ON	0

Transfer characteristics :-



⇒ lowest power dissipation.

P_{diss} = 0.01 mw

t_{pd} = 70 nsec

PDM = 0.7 pJ

Fanout = 50

NM = $\frac{V_{DD}}{2}$

Power Dissipation :-

(i) Static PD =

(a) During logic '0' or logic '1'.

(ii) Dynamic PD =

During transition from 0→1 or 1→0.

$$PD = Cf V_{DD}^2$$

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