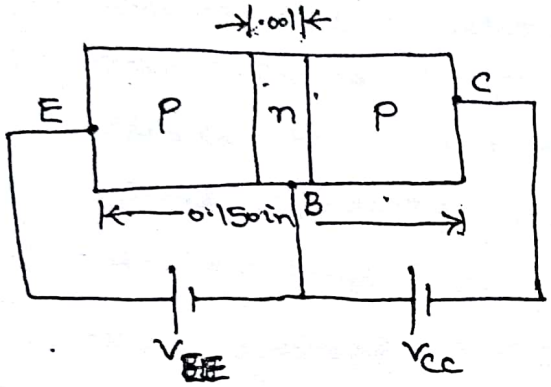
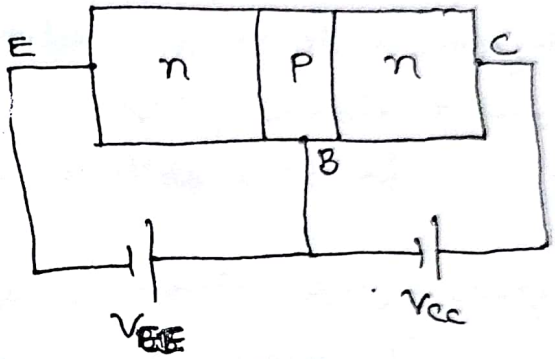
Transistor: The transistor is a three layer semiconductor device consisting of either two n and one P-type layers of material (or) two P and one n-type layer of material.

The former is called an n-P-n transistor, while the later is called a P-n-P transistor.



P-n-P Transistor



n-P-n Transistor

D.C Biasing is necessary to establish the proper region of operation for a.c amplification.

The emitter layer is heavily doped, the base is lightly doped and the collector is heavily doped but less than emitter (or we can say that collector is moderately doped).

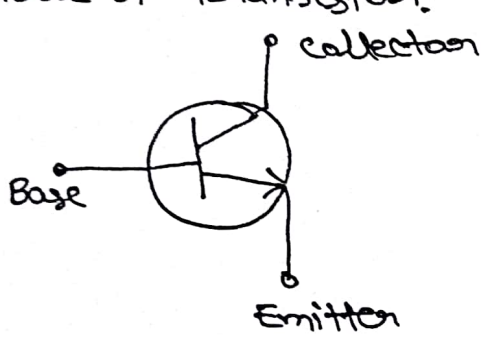
For the Transistor shown above the ratio of the total width to that of the central layer is $0.150 / 0.001 = 150:1$

The doping of the central layer (sandwiched layer) is also considerably less than that of the outer layers. This lower doping level decrease the conductivity (increase the resistance) of this material by limiting the number of free carriers.

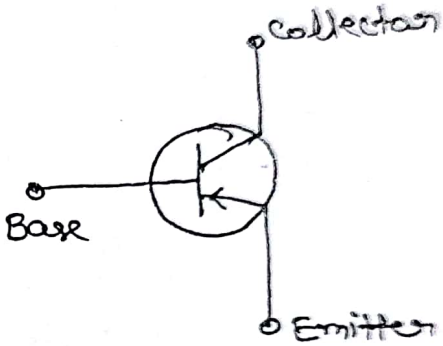
For the biasing shown above, the terminal have been indicated by the capital letters, E for Emitter, C for Collector, and B for Base.

The abbreviation BJT, from bipolar junction transistor is often applied to this three terminal device. The term bipolar reflects the fact that holes and electrons participate in the injection process into the oppositely polarized material.

Symbol of Transistor:



N-P-N Transistor



P-N-P Transistor.

Transistor in unbiased condition (or) Unbiased Transistor:

When no supply is connected to a transistor, the transistor is in unbiased condition.

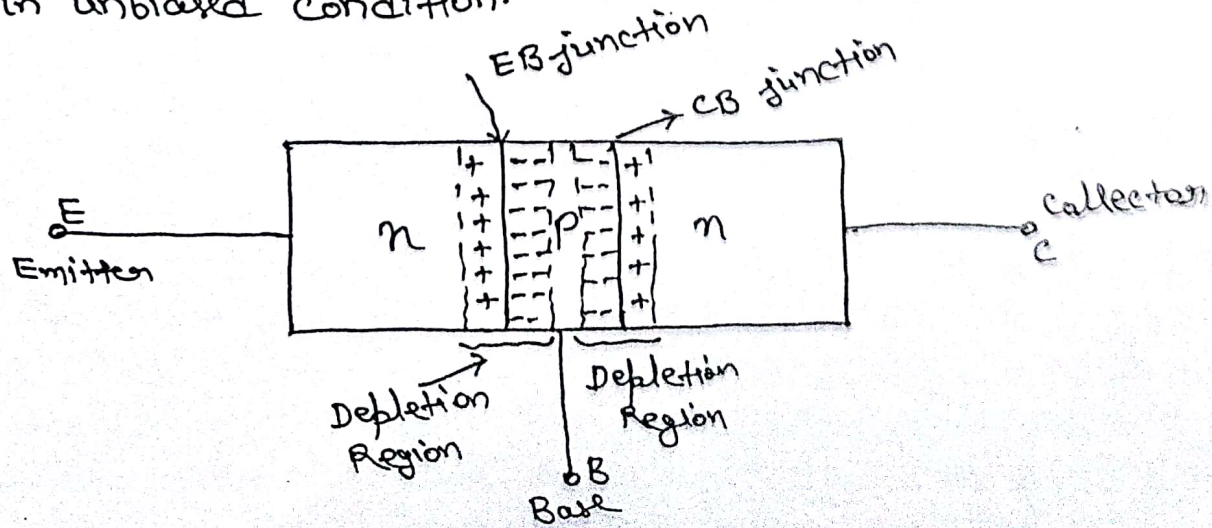


Figure shows the depletion region formation of transistor, when the transistor is unbiased.

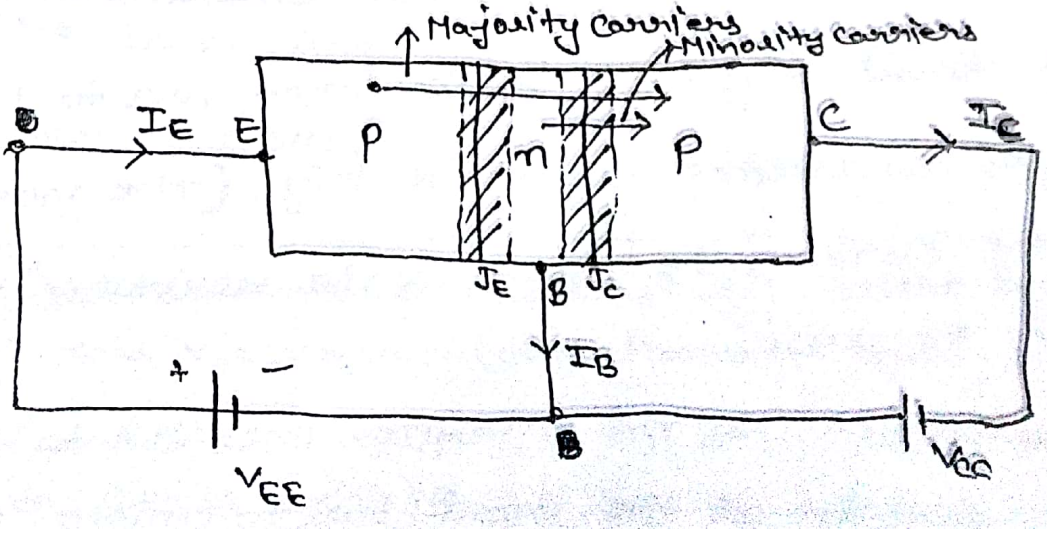
In this case, the diffusion of charge carriers across the junction produces two depletion regions. The width of depletion region is not same on both sides of junction because of different doping levels of the transistor.

The depletion region penetrates more in lightly doped region. Therefore penetration of depletion region is less in the heavily doped collector and emitter regions and more in the base region.

Transistor operation (P-N-P):

The Basic operation of the transistor can be described using P-n-P (or) n-P-n transistor. The operation of the n-P-n transistor is exactly the same if the roles played by the electron and holes are interchanged.

* one P-n junction of transistor is forward biased while the other is reverse biased.



Consider a P-n-P transistor with biasing potential as shown in the fig.

As shown in fig., the Emitter-Base junction is forward biased and collector-base junction is reverse biased So, that the width of depletion region will be more at collector-base junction.

A large number of majority carriers will diffuse across the forward biased P-n junction into the n-type material. Since the n-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal.

The Magnitude of the base current is typically on the order of microamperes as compared to milliampere for the emitter and collector currents.

The large number of these majority carriers will diffuse across the reverse-biased junction into the P-type material connected to the collector terminal.

Applying Kirchoff's current law to the transistor, we obtain

$$I_E = I_C + I_B$$

Emitter current is the Sum of the collector and Base Current.

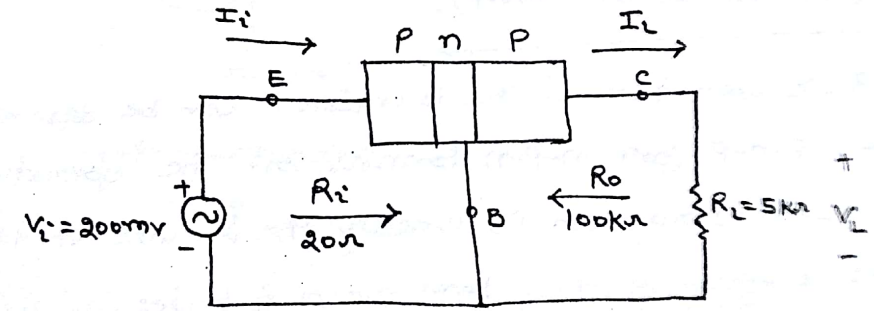
The collector current is comprised of two components the majority and minority carriers. The minority current component is called the leakage current and is given by I_{CO}.

The Relationship between I_C and I_E has been established during transistor configuration, which is

$$I_E = I_B + I_C$$

(OR) $\boxed{I_E \simeq I_C}$

The basic Amplifying Action of the transistor can be introduced on a surface level using the network as shown in fig.



For the common base configuration the ac input resistance is determined by the Input characteristics, which is very small, typically varies from 10Ω to 100Ω. The output resistance is quite high (the more horizontal is the curves, the higher is the resistance), varies from 50KΩ to 1MΩ.

The difference in the resistance is due to the forward biased junction at the input (base to emitter) and reverse

biased at output (base to collector) junction.

$$I_i = \frac{V_i}{R_i} = \frac{200mV}{20\Omega} = 10mA$$

If we assume for the moment that $I_C = I_E$
it means $\alpha_{ac} = 1$

$$I_L = I_i$$

[Because $I_L = I_C$, $I_E = I_i$]

and $V_L = I_L R_L$

$= (10mA)(5K\Omega)$

$V_L = 50V$

The voltage Amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50V}{200mV} = 250$$

* Typical value of voltage Amplification for the common base configuration vary from 50 to 300.

* The current Amplification is always less than 1. (α

NOTE: The Basic Amplifying action was produced by transf
the Source current I_i from low to a High Resistan
Circuit.

Example: calculate the voltage Gain ($A_v = \frac{V_L}{V_i}$), for the figure (as above)
If $R_L = 1K\Omega$ and $V_i = 400mV$. (other Parameter Remain same).

Example: calculate voltage gain, if the Source has an internal resi
of 100Ω in Series with V_i.

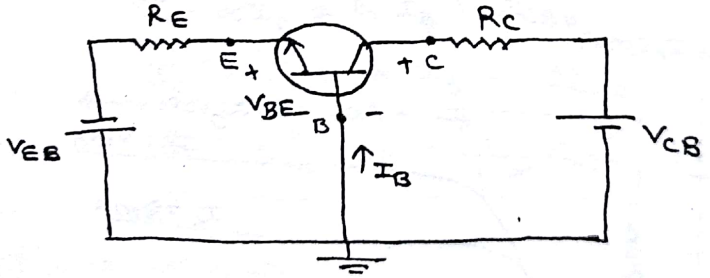
Transistor configuration:

Depending on which terminal is made common to Input and output terminal, there are three possible configuration of the transistor.

1. Common Base configuration.
2. Common Emitter configuration.
3. Common Collector configuration.

Common Base configuration:

The common Base terminology derived from the fact that the base is common to both the Input and output sides of the configuration.

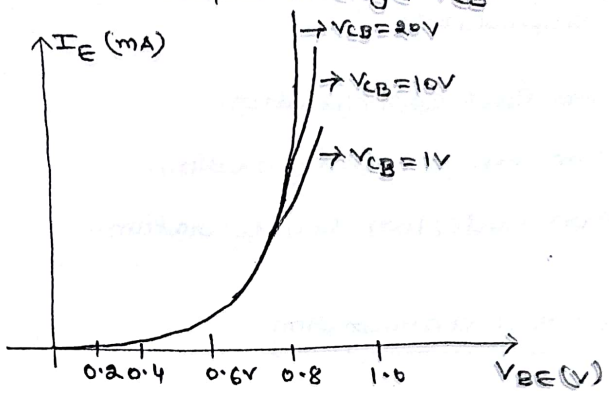


The arrow in the graphical symbol defines the direction of emitter current through the device.

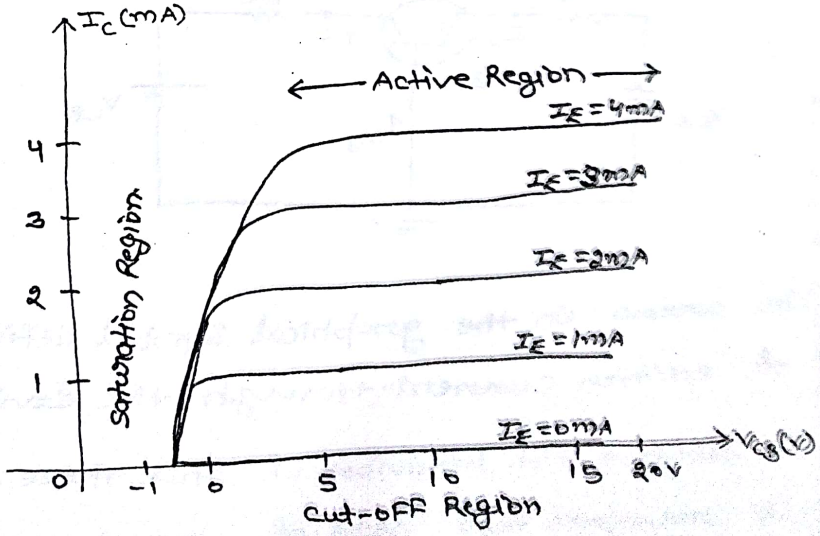
To describe the behavior of this three terminal device, it requires two sets of characteristics.

1. Input characteristic (or) driving point characteristics.

The Input set of common Base characteristics relates the Input current I_E to an Input voltage (V_{BE}), for various levels of output voltage V_{CB}.



The output set relates an output current (I_C) to an output voltage (V_{CB}) for various level of input current I_E as shown in fig.

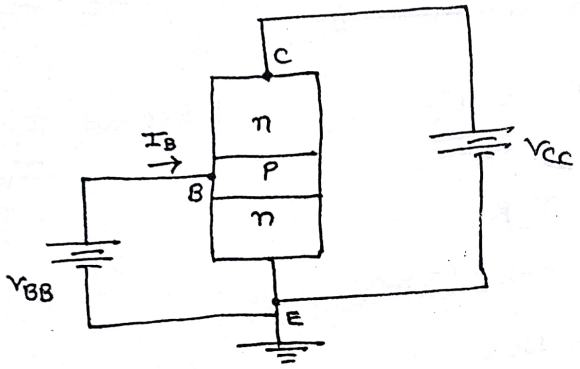


The output (or) collector set of characteristics has three basic region of interest.

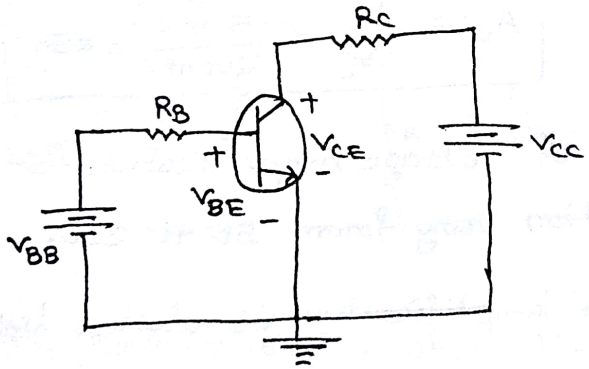
1. Active Region
2. cut-off Region

Common Emitter Configuration:

The most frequently encountered transistor configura is common Emitter configuration. (Emitter is common to Base and collector terminal).



And similarly, we can draw CE configuration with transistor symbol.



Two sets of characteristics are necessary to describe the behavior of common Emitter Configuration.

→ one for the base Emitter Circuit

→ one for the collector-Emitter Circuit.

Current Gain 'α' :

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called alpha, and defined by:

$$\alpha_{dc} = \frac{I_C}{I_E} \qquad \alpha < 1$$

And $\boxed{I_C = \alpha_{dc} I_E}$

But, As we Know

$$I_{C_{Total}} = I_{C_{maj.}} + I_{C_{min.}}$$

$$\boxed{I_C = \alpha I_E + I_{CBO}}$$

The Active Region is defined by the Biasing arrangement. At the Lower end of the Active Region $I_E = 0mA$, and I_C is simply due to the reverse Saturation current I_{CBO}. And I_{CBO} is very low for general purpose (silicon) transistor. So, it can be neglected.

But, As we Know Reverse Saturation current is highly Sensitive to temperature, At Higher temp., the effect of I_{CBO} is a important factor.

So that $\boxed{I_C \simeq I_E}$ (In Active Region)

→ The cut-OFF Region (Both junction Reverse Biased) is defined that region where $I_C = 0A$.

→ The Saturation Region (Both junction forward Biased) is to

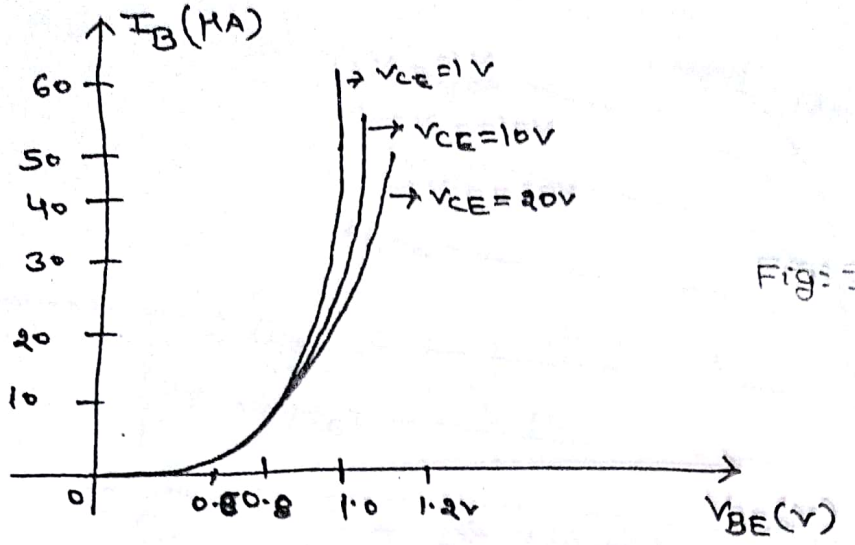


Fig: Input characteristics

The output characteristics can be drawn with the help of output current equation.

As we know From common Base configuration

$$I_C = \alpha I_E + I_{CBO} \quad -- (i)$$

$I_E = I_B + I_C$ Put in (i)

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}}$$ --- For CE configuration

If we consider

$I_B = 0A$

$$I_C = \frac{1}{1-\alpha} I_{CBO}$$

As we know $\alpha < 1$, Assume $\alpha = 0.996$

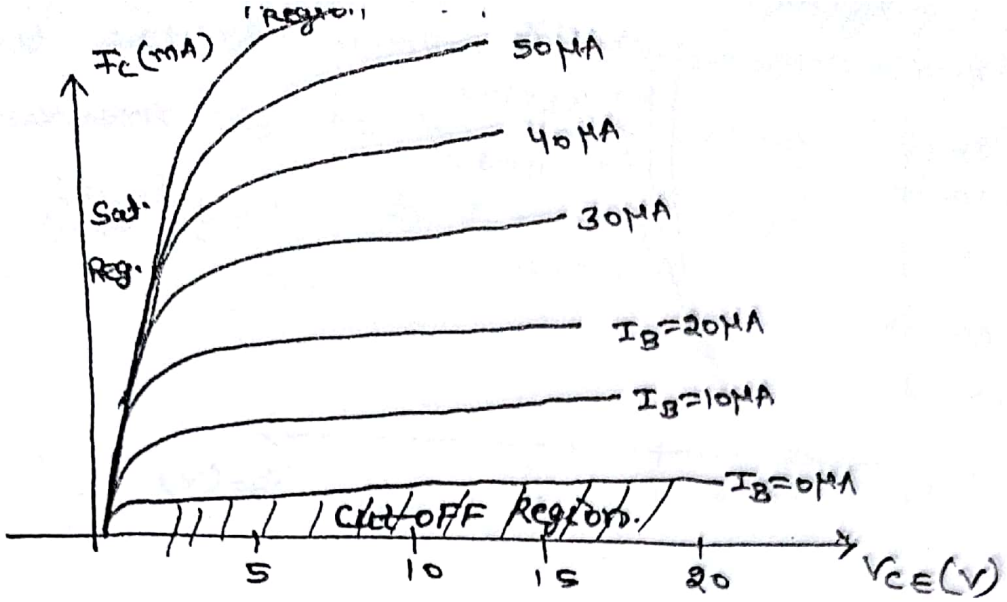
$$I_C = \frac{1}{1-0.996} I_{CBO}$$

$$I_C = 250 I_{CBO}$$

I_{CBO} = Reverse Sat. current, Assume $I_{CBO} = 1\mu A$

It means $I_C = 250\mu A$ when $I_B = 0A$.

ue to this factor, there is some slope in output char.



Current Gain β_{dc}:

$$\beta_{dc} = \frac{I_C}{I_B} \qquad \beta > 1$$

And $\boxed{I_C = \beta_{dc} I_B}$

Relation Between α and β.

$$\alpha = \frac{I_C}{I_E}, \quad \beta = \frac{I_C}{I_B}$$

$$I_E = I_C + I_B$$

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \beta = \alpha\beta + \alpha$$

$$\beta = (\beta+1)\alpha$$

$$\boxed{\alpha = \frac{\beta}{\beta+1}} \quad \text{And} \quad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

And Recall CE output current eqn

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

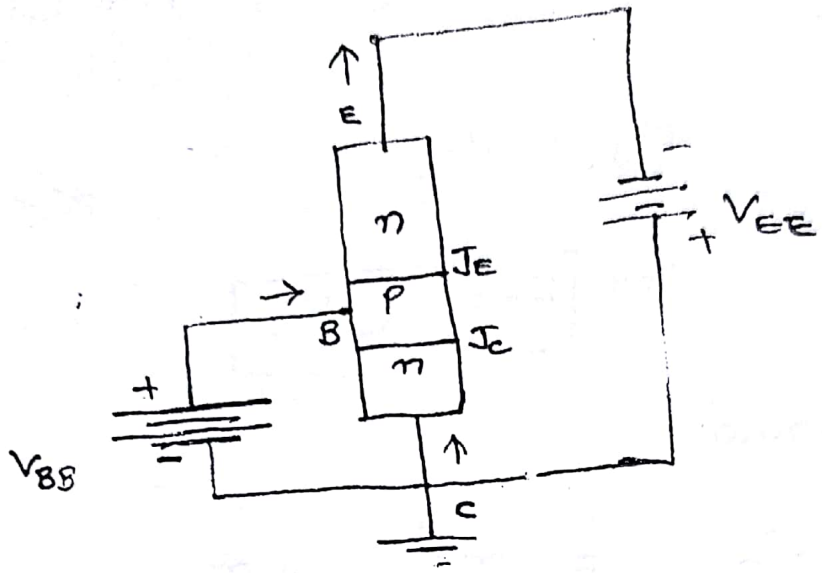
$$I_C = \beta I_B + \underbrace{(\beta+1) I_{CBO}}_{I_{CEO}}$$

(OR)

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

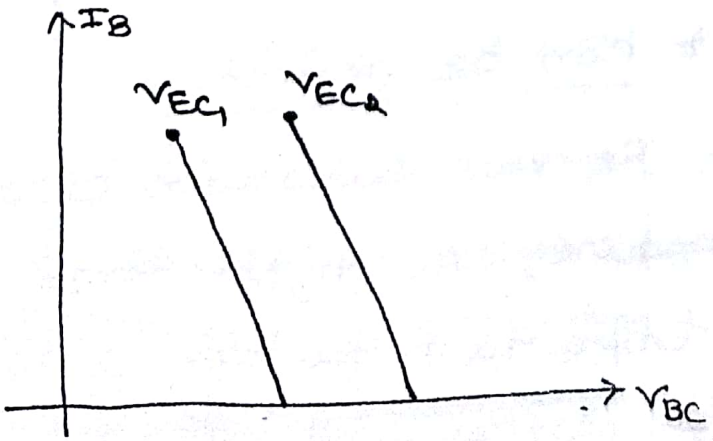
....mon collector configuration:

The common collector configuration with proper current and voltage direction is shown in fig.



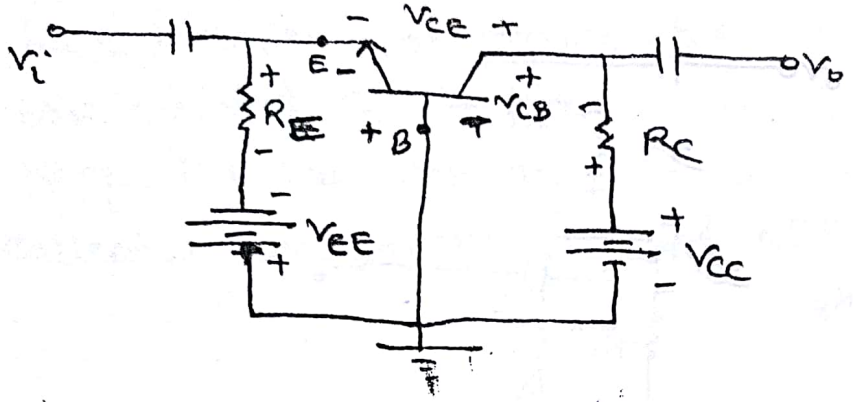
The common collector configuration is used primarily for impedance matching purpose, since it has a high Input impedance and low output impedance, opposite to that of common base and common Emitter configuration.

The Input characteristics graph plotted between base current I_B and Input voltage V_{BC} while maintaining output voltage V_{EC} constant.



The output characteristics is a graph plotted between output

Common Base configuration:



$$-V_{EE} + I_E R_E + V_{BE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$I_E \simeq I_C$$

$$V_{CE} = V_{EE} + V_{CC} - I_E (R_C + R_E)$$

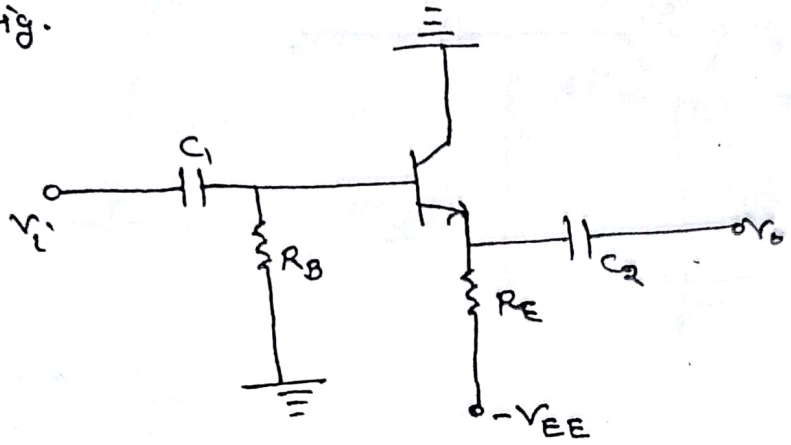
$$V_{CB} + I_C R_C - V_{CC} = 0$$

$$I_C \simeq I_E$$

$$V_{CB} \simeq V_{CC} - I_C R_C$$

Emitter - Follower configuration:

This section will examine a configuration where the output is taken off the emitter terminal as shown in fig.



By Applyin KVL in the Input circuit

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

By using $I_E = (\beta+1) I_B$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta+1) R_E}$$

For the output network, Applying KVL

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

Problem: $R_B = 240K\Omega$, $\beta = 90$, $R_E = 2K\Omega$ $V_{EE} = -20V$, Determine V_{CE_Q}, and I_{E_Q}.

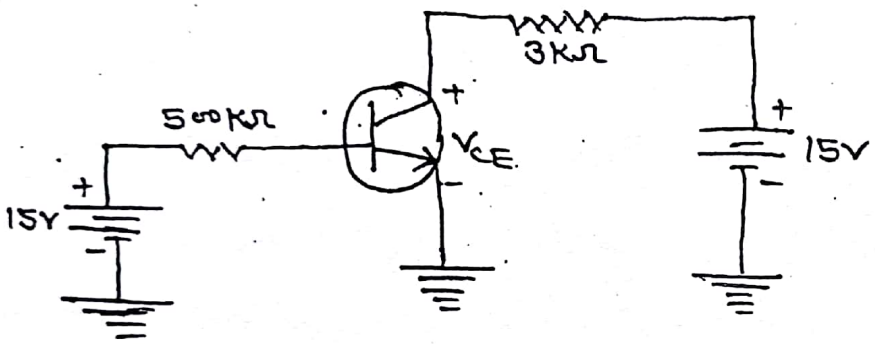
Solution: $I_B = 45.73\,\mu A$, $V_{CE_Q} = 11.68V$, $I_{E_Q} = 4.16mA$

...ic operating point

Every transistor circuit has a load line. When any circuit is given, find out the value of saturation current and the cut-off voltage. Then, these values are plotted on the vertical and horizontal axes. Then draw a line through these two points to get the load line.

Plotting the Q-Point:

Below figure shows a base-biased circuit with a base resistance of 500KΩ.



First, we will visualize a short across the collector emitter terminal ($V_{CE} = 0$)

$$V_{CE} = V_{CC} - I_C R_C$$

$$0 = V_{CC} - I_C R_C \Rightarrow I_C = \frac{V_{CC}}{R_C} = \frac{15}{3K\Omega} = 5mA$$

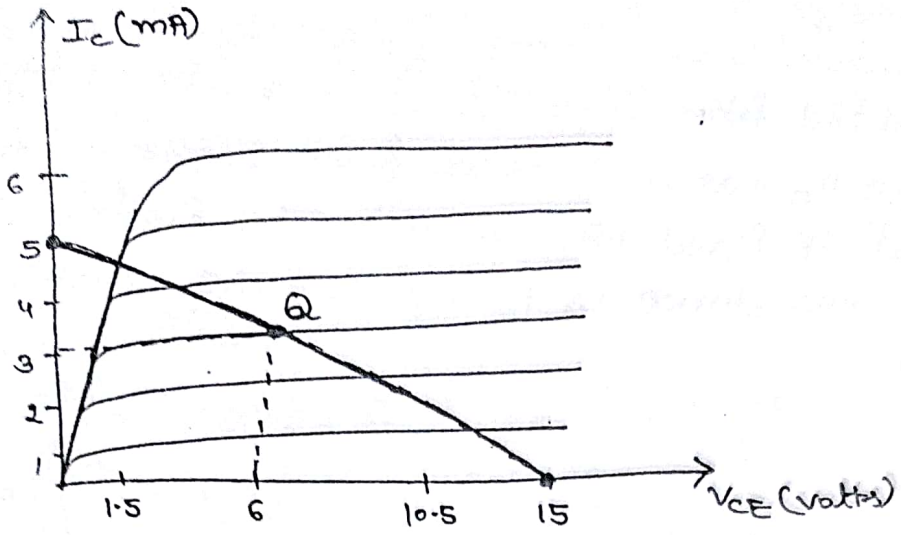
$$\boxed{I_{C\,sat.} = 5mA}$$

Second, visualize the collector-emitter terminal is open ($I_C = 0$)

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} = 15V \Rightarrow \boxed{V_{CE\,(cut-off)} = 15V}$$

It means all the supply voltage appears across the collector-emitter terminals.



Now, Assume that, the transistor is ideal, it means that

$$V_{BE} = 0V.$$

This means that all the base supply voltage will appear across the base resistor.

Therefore, the base current is

$$I_B = \frac{15V}{500k\Omega} = 30\mu A.$$

Assume that current gain (β) of the transistor is 100.

$$\beta = 100$$

Then the collector current is

$$I_C = 100\,(30\mu A) = 3mA.$$

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 15 - (3mA)(3k\Omega) = 6V.$$

By plotting 3mA and 6V (the collector current and voltage) we get the operating point labeled as Q in the figure. and also called as the quiescent point.

Other types of Bias:

1. Fixed Bias circuit:

Below figure shows the fixed Bias circuit for NPN transistor. A high resistance R_B is connected between supply V_{cc} and base terminal of transistor. The Required zero signal base current 'I_B' is provided by V_{cc}. A single supply V_{cc} keeps the base emitter junction forwoord biased and the collector base junction reverse biased.

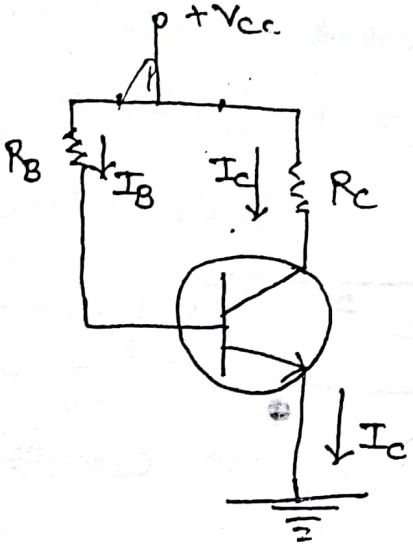
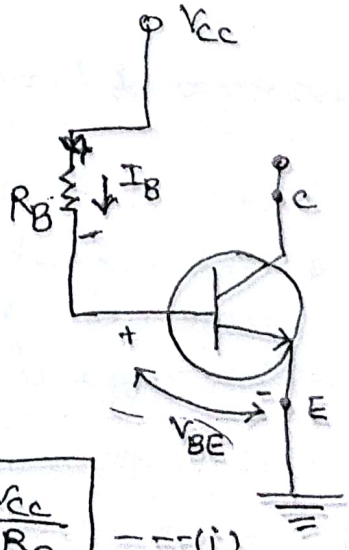


fig: Fixed Bias circuit

Analysis of fixed Bias circuit:

(i) Base circuit:



By Applying KVL to the base circuit

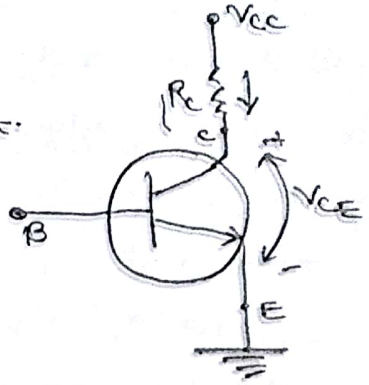
$$V_{cc} - I_B R_B - V_{BE} = 0$$

The Base current is given by

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} \approx I_B \approx \frac{V_{cc}}{R_B} \quad ---(i)$$

The Supply voltage V_{cc} is of fixed value. once the resistance R_B is selected, I_B is also fixed. Hence this circuit is called.

(ii) Collector circuit:



By Applying KVL to the collector circuit.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \quad -- (ii')$$

and $$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}} \quad --- (iii')$$

The collector current in CE configuration is given as:

$$I_C = \beta I_B + I_{CEO}$$

$$\beta I_B >> I_{CEO}$$

$$\boxed{I_C \simeq \beta I_B} \quad --- (iv)$$

$$V_{CE} = V_C - V_E \quad] \; V_{CE} = V_C$$

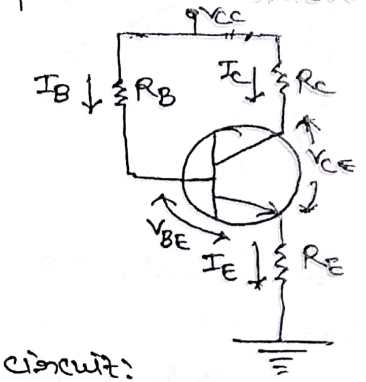
Equations (i), (ii') and (iii') corresponds to operating points I_{BQ}, I_{CQ} and V_{CEQ} respectively.

Advantages of fixed Bias circuit:

1. It is a simple circuit which uses few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by changing value of R_B.

Disadvantages of fixed Bias circuit:

The modified fixed Bias circuit is shown in figure be
Resistance R_E has been added from emitter to the ground
terminal of fixed bias circuit. The Purpose of adding
emitter resistance is to improve the stability of the
circuit.



Analysis of modified fixed Bias circuit:

(i) Base circuit:

By applying KVL to the base circuit.

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

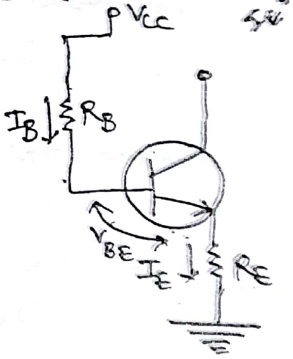
But

$$I_E = I_B + I_C$$

and $I_C = \beta I_B$

$$I_E = I_B + \beta I_B$$

$$= I_B(\beta + 1)$$



$$V_{CC} = I_B R_B + V_{BE} + (\beta I_B + I_B) R_E$$

$$= I_B R_B + V_{BE} + \beta I_B R_E + I_B R_E$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_E + R_E}}$$

(ii) Collector circuit:

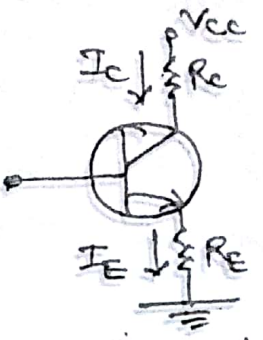
By applying KVL to collector circuit.

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \qquad \therefore I_E = I_B + I_C$$

$\therefore I_B << I_C$

$$V_{CE} = V_{CC} - I_B R_E - I_C (R_C + R_E)$$

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$



$$I_C = \beta I_B$$

Put the value of I_B from base circuit analysis

$$I_{CQ} = \beta \frac{V_{CC} - V_{BE}}{R_B + \beta R_E + R_E}$$

Collector to Base Bias circuit:

Below figure shows the collector to base bias circuit. It is an improvement over the fixed bias circuit. In this biasing circuit one end of resistor R_B is connected to the base and other end to the collector.

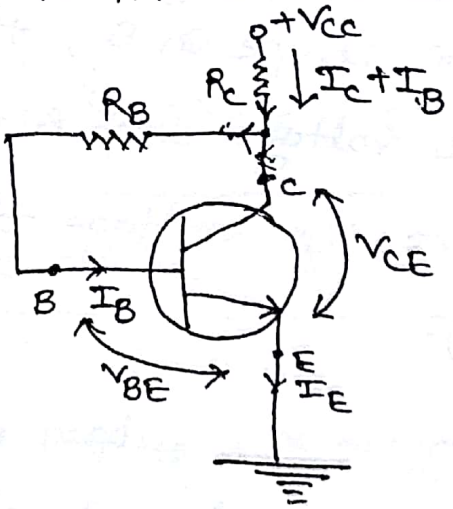
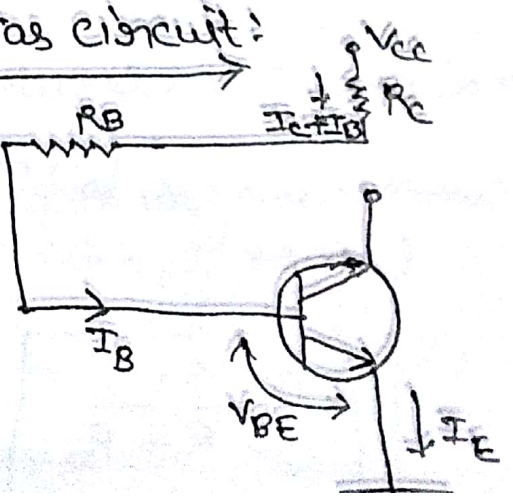


Fig: Collector to Base Bias circuit

Analysis of collector to Base-Bias circuit:



(i) Base circuit:

Applying KVL to the Base circuit

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_C R_C + I_B R_C + I_B R_B + V_{BE}$$

We know $I_C = \beta I_B$

So, that

$$V_{CC} = \beta I_B R_C + I_B R_C + I_B R_B + V_{BE}$$

$$= I_B \left[(1+\beta) R_C + R_B \right] + V_{BE}$$

∴ The Base current is

$$I_B = \frac{V_{CC} - V_{BE}}{(1+\beta) R_C + R_B}$$

Base current at Q-point

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{(1+\beta) R_C + R_B} \quad \text{---(i')}$$

(ii') collector-circuit:

By applying KVL to the circuit

$$V_{CC} = (I_C + I_B) R_C + V_{CE}$$

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

collector-emitter voltage at point Q

$$V_{CEQ} = V_{CC} - (I_C + I_B) R_C$$

$$I_C = \beta I_B$$

collector current at point Q

$$I_{CQ} = \beta I_{BQ}$$

By Substituting value of I_{BQ}

$$I_{CQ} = \frac{\beta (V_{CC} - V_{BE})}{(1+\beta) R_C + R_B}$$

If there is a change in β due to replacement by a same type of transistor, (or) there is a change in β due to the change in temperature, then collector

current I_C will increase- ($\because I_C = \beta I_B$)

As a Result voltage drop across R_C increase ($V_C = I_C R_C$)

Since Supply voltage V_{CC} is constant, due to increase in $I_C R_C$, the value of V_{CE} decrease.

Due to Reduction in V_{CE}, I_B will reduces, because

$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

$$(I_C + I_B) R_C = V_{CC} - V_{CE}$$

$$I_C R_C + I_B R_C = V_{CC} - V_{CE}$$

$$I_B R_C = \frac{V_{CC} - V_{CE}}{} - I_C R_C$$

$$I_B = \frac{V_{CC} - V_{CE} - I_C R_C}{R_C}$$

As I_C depends on I_B,

$$I_C = \beta I_B$$

It will decrease the value of I_C.

The result is that circuit tends to maintain stable value of collector current, keeping the Q-point fixed.

Advantages: 1. It is a simple biasing circuit

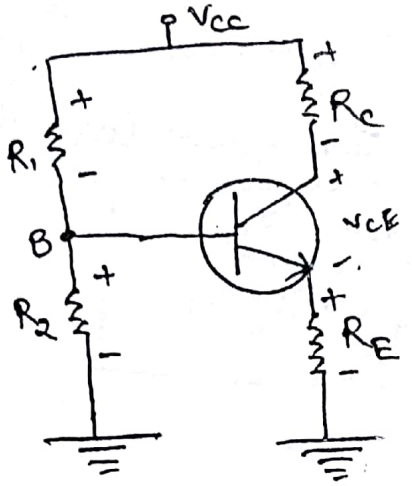
2. This circuit provides some stabilization of operating

Disadvantages: 1. The circuit does not provide good stabilization because Stability factor is high. (lesser than fixed bias).

2. This circuit arrangement provides a negative feedback which

Voltage Divider Bias:

Figure shows the most widely used biasing circuit. Now the base circuit contain a voltage divider (R_1 and R_2). Because of this, the circuit is called voltage-Divider Bias.



In this circuit biasing is provided by three resistors R_1, R_2 and R_E. The Resistor R_1 and R_2 acts as a potential divider giving a fixed voltage to point B, which is base.

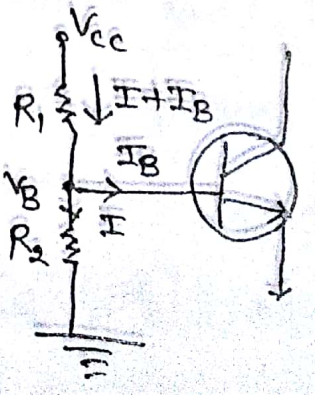
If collector current changes (or) increase due to change in temperature (or) change in β, the emitter current also increase and voltage drop across R_E increase, and this will reduce the voltage difference between base and emitter (V_{BE}).

Due to Reduction in V_{BE}, base current I_B and hence collector current I_C also reduces.

Analysis- Base circuit:

Current across loop (when $I_B = 0$)

$$I = \frac{V_{cc}}{R_1 + R_2}$$

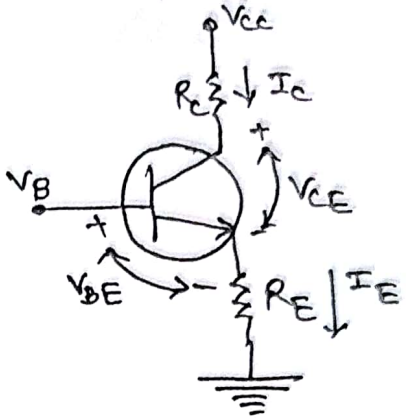


voltage drop across $R_2 = V_B$

$$V_B = \frac{V_{CC} * R_2}{R_1 + R_2}$$

[By voltage-Divider]

Collector-circuit:



voltage drop across R_E can be obtained as

$$V_E = I_E R_E = V_B - V_{BE}$$

(or)

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

$I_E \simeq I_C$

So, $I_C \cong \frac{V_B - V_{BE}}{R_E}$

Applying KVL to the collector circuit, we get

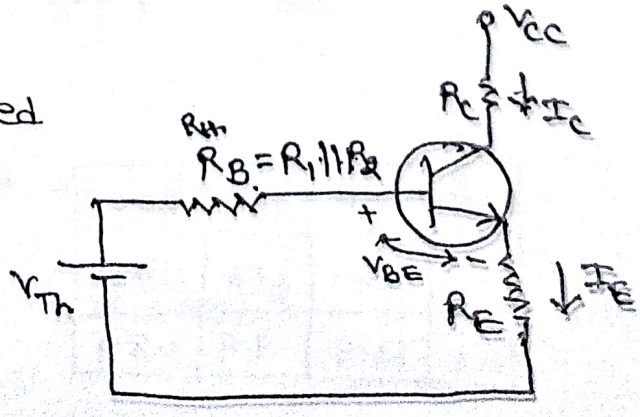
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

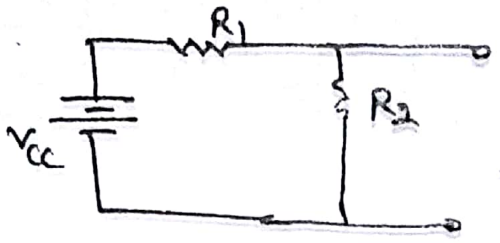
Accurate Voltage Divider Bias Analysis (or) Simplified circuit of voltage Divider Bias.

Figure shows the simplified circuit of voltage divider bias. Here R_1 and R_2 are replaced by R_B and V_T

$R_D = R_1 \| R_2$



V_{th} = Thevenin voltage



$R_{th} \equiv R_1 \| R_2$

$V_{th} \equiv \frac{V_{CC} * R_2}{R_1 + R_2}$

Applying KVL to Base circuit.

$$+V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$I_E = (\beta+1) I_B$ → Put in above eqn

we get, $$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta+1) R_E}$$

As we know $\beta = \frac{I_C}{I_B}$

$$I_C = \beta I_B$$

Applying KVL at collector side

$$+V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

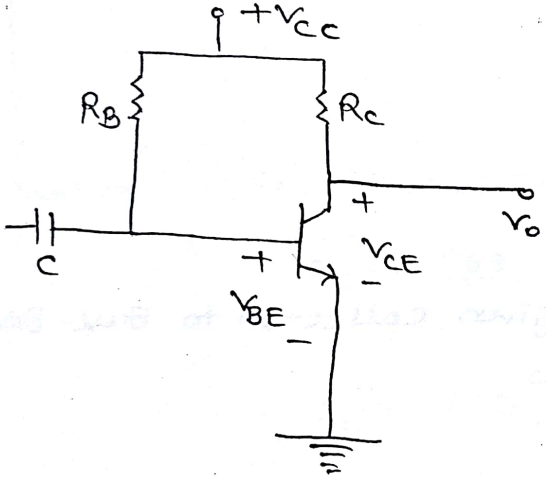
$I_E \simeq I_C$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Amplifier:

Amplifier: An Electronic circuit which increases the strength of weak electrical signal without changing its shape.

Amplification = Amplitude + Magnification



As we know, the given circuit is Fixed-Bias configuration,

$$+V_{CC} - V_{BE} - I_B R_B = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{20V - 0.7V}{1000K\Omega}$$

$$I_B = 19.3\mu A \simeq 20\mu A$$

As we know, $I_C = \beta I_B$

$$I_C = 100 \times 19.3\mu A = 1.93mA \simeq 2mA$$

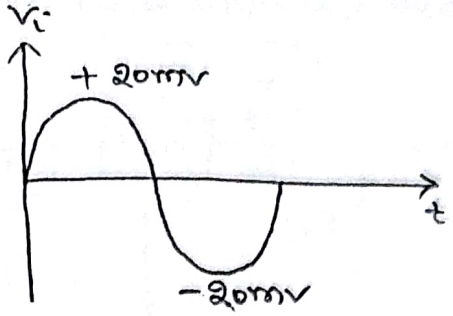
$$V_{CE} = V_{CC} - I_C R_C$$

$$= 20V - 1.93mA * 5K\Omega$$

$$V_{CE} = 10.15V \simeq 10V$$

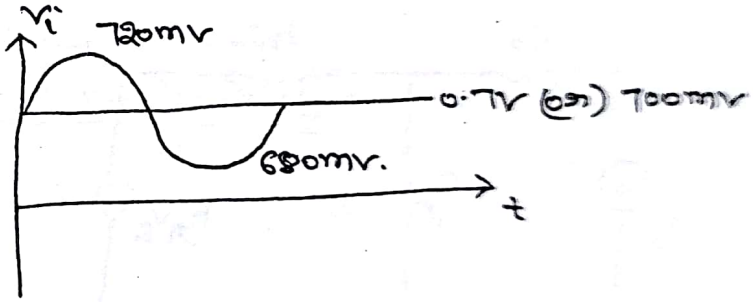
Let v_i be a sine wave whose values varying from +20mv to −20mv.

v_i = AC Input to the Amplifier.

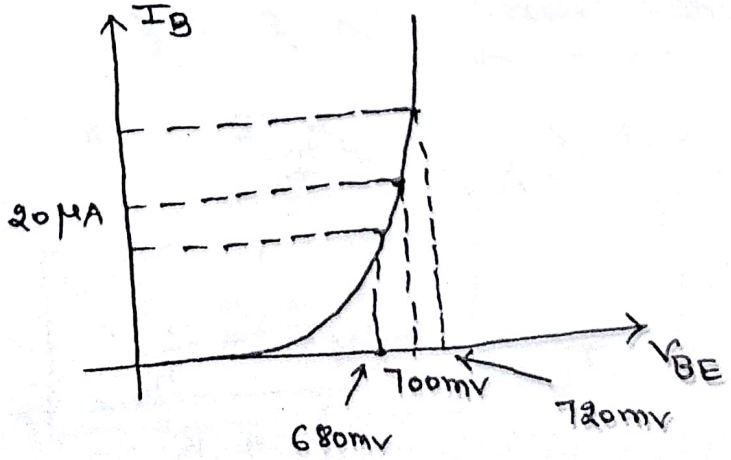


The Applied AC Input gets super-imposed on the DC voltage present between base and emitter.

* Due to this net V_{BE} will vary sinusoidally from 680 mv to 720 mv.



Due to variation in V_{BE}, base current will vary.



Let the variation in base current be ± 2μA

$\Delta I_B = \pm 2\mu A$

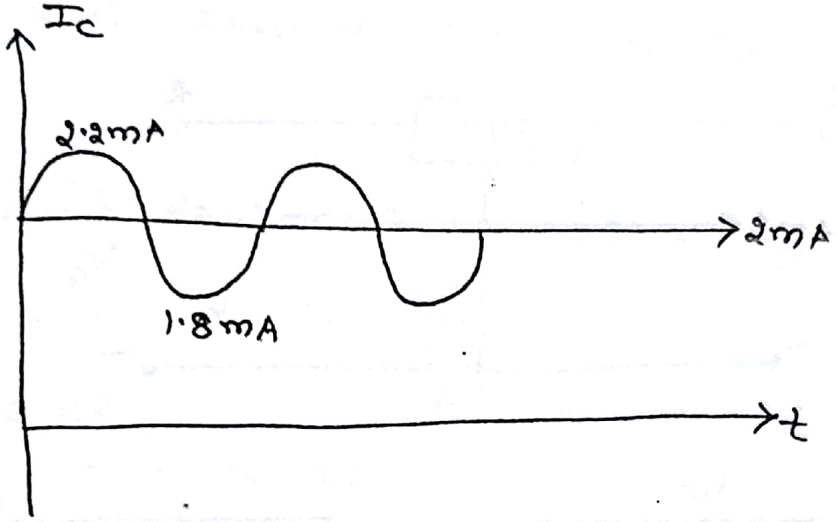
Due to variation in I_B, collector current also varies.

$$I_c = \beta I_B$$

$$\Delta I_c = \beta \cdot \Delta I_B$$

$$= 100 * (\pm 2\mu A)$$

$$\Delta I_c = \pm 0.2mA.$$



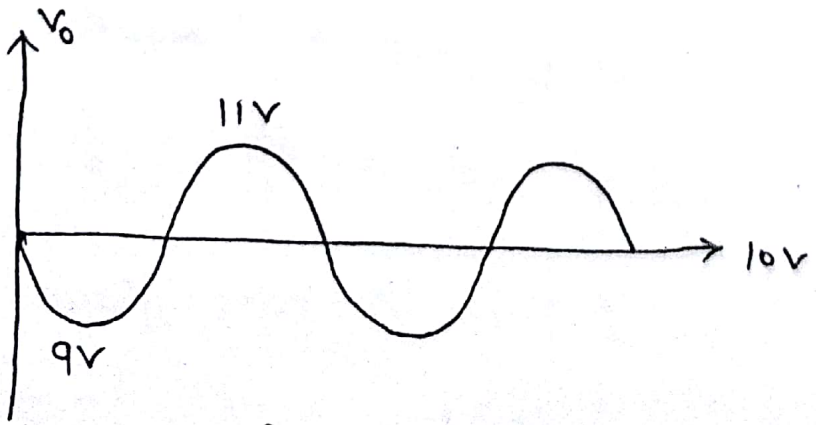
Due to change in I_c, V_{CE} (or) V_o changes and,

$$V_o = V_{CE} = V_{cc} - I_c R_c$$

$$\Delta V_o = 0 - \Delta I_c R_c$$

$$= \mp 0.2 * 5$$

$$= \mp 1V$$



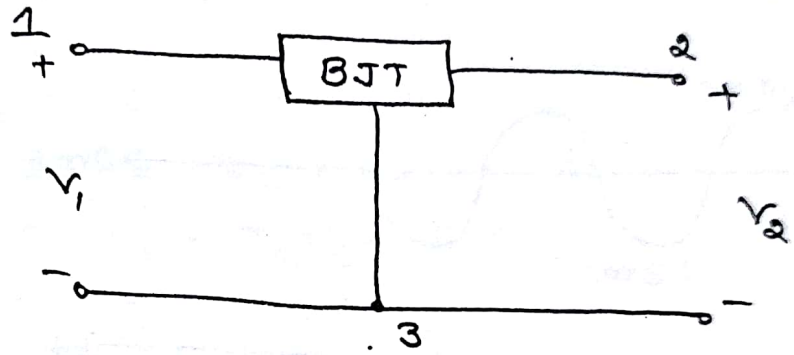
E: A Peak change of 20mV in the Input voltage creates a peak inge of 1V in o/p voltage (voltage Amplification is 50 times) with, 180° Phase shift.

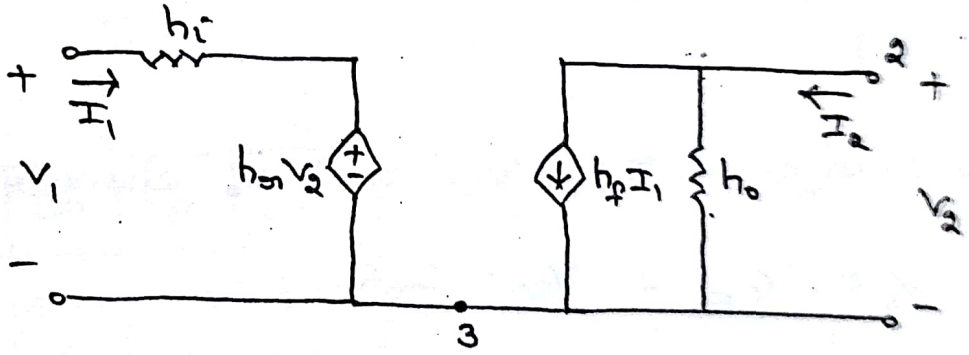
H- Parameter (or) Hybrid Parameter model:

It is obtained from H-parameter equations.

$$V_1 = h_i I_1 + h_r V_2 \quad \text{---(i)}$$

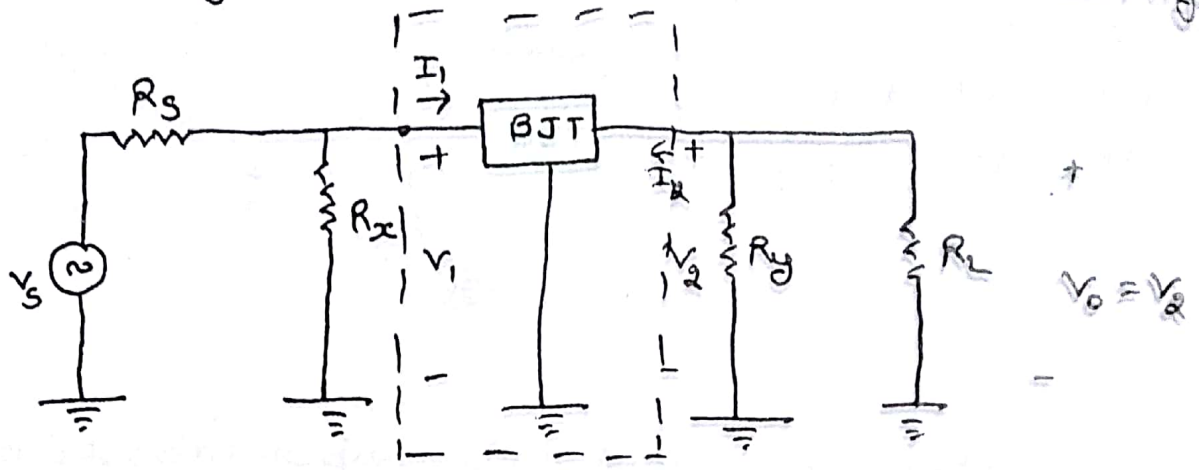
$$I_2 = h_f I_1 + h_o V_2 \quad \text{---(ii)}$$



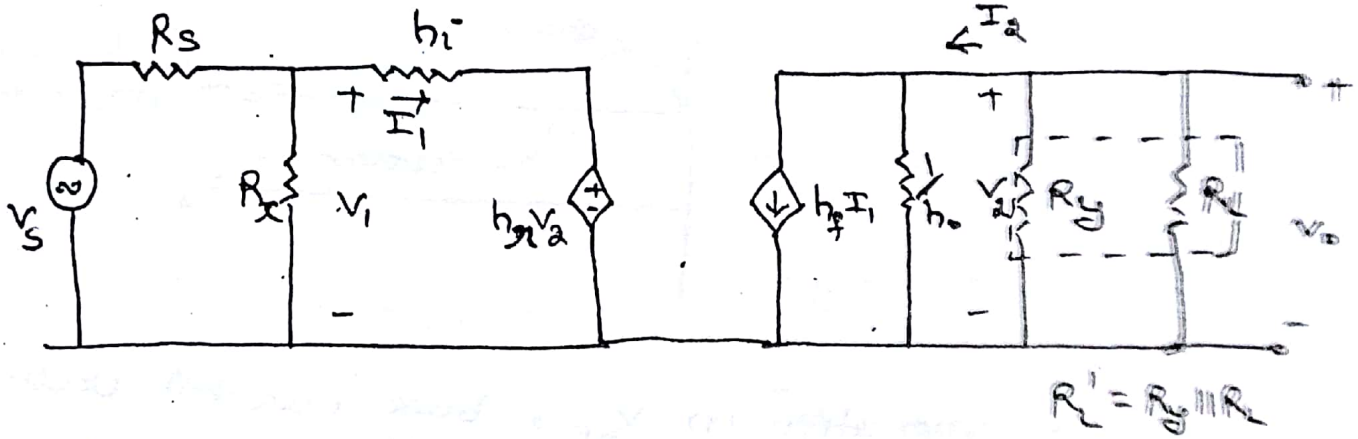


General BJT Amplifier Analysis:

This Analysis is Applicable to all three configurations



To Analyze the amplifier, circuit should be redrawn by replacing BJT with H- parameter model.



1) Current Gain:

$$A_I = \frac{I_L}{I_1}$$

$$I_L = \frac{-h_f I_1 * \frac{1}{h_o}}{\frac{1}{h_o} + R_L'} \Rightarrow \frac{-h_f I_1}{1 + h_o R_L'}$$

$$\boxed{A_I = \frac{I_L}{I_1} = \frac{-h_f}{1 + h_o R_L'}}$$

2. Input Resistance : R_i

$$R_i = \frac{V_1}{I_1}$$

By Applying KVL at I/P side.

$$+V_1 - I_1 h_i - h_r V_2 = 0$$

$$V_1 = h_i I_1 + h_r V_2 \qquad [\because V_o = V_2,\ V_2 = I_L R_L']$$

$$V_1 = h_i I_1 + h_r I_L R_L'$$

$$V_1 = h_i I_1 + h_r A_I I_1 R_L' \qquad [A_I = \frac{I_L}{I_1},\ I_L = A_I I_1]$$

$$\frac{V_1}{I_1} = h_i + h_r A_I R_L'$$

$$\boxed{R_i = h_i + h_r A_I R_L'}$$

3. Voltage Gain:

$$A_V = \frac{V_2}{V_1}$$

$$V_2 = I_L R_L'$$

$$A_V = \frac{I_L R_L'}{V_1} = \frac{A_I I_1 R_L'}{V_1}$$

$$\boxed{A_V = A_I * \frac{R_L'}{R_i}}$$

NOTE:
(i) $A_I = \frac{I_L}{I_1}$
$I_L = A_I$
(ii) $R_i =$

1. Output Resistance: R_o

Assumption:

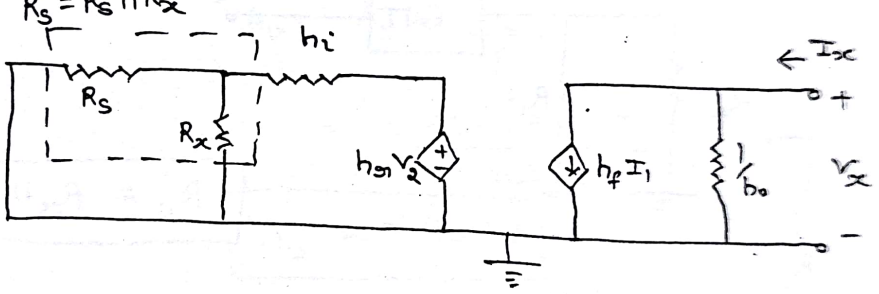
i) Disable External source present in the circuit.

ii) Disconnect Load Res. R_L'

iii) ~~Assume~~ Apply External voltage V_x at the output port and Assume current I_x flows into output port.

Then output Resistance is defined as:

$$R_o = \frac{V_x}{I_x}$$



Apply KCL at node 2.

$$I_x = h_o V_x + h_f I_1 \qquad \left[\frac{V_x}{1/h_o} = h_o V_x\right]$$

Divide both side by V_x

$$\frac{1}{R_o} = \frac{I_x}{V_x} = h_o + h_f \frac{I_1}{V_x} \qquad \text{---- (i)}$$

Apply KVL in Loop 1.

$$-I_1 R_s' - h_i I_1 - h_r V_x = 0$$

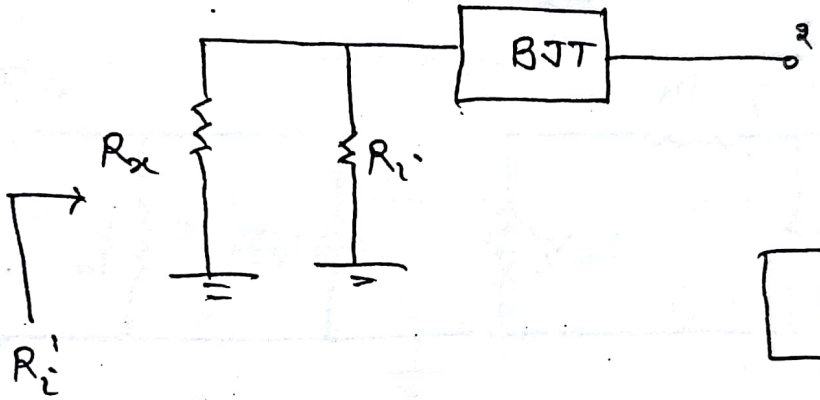
$$I_1 (R_s' + h_i) = -h_r V_x$$

$$\frac{I_1}{V_x} = \frac{-h_{rf}}{R_s' + h_i} \quad \text{---(ii)}$$

Put (ii) in (i)

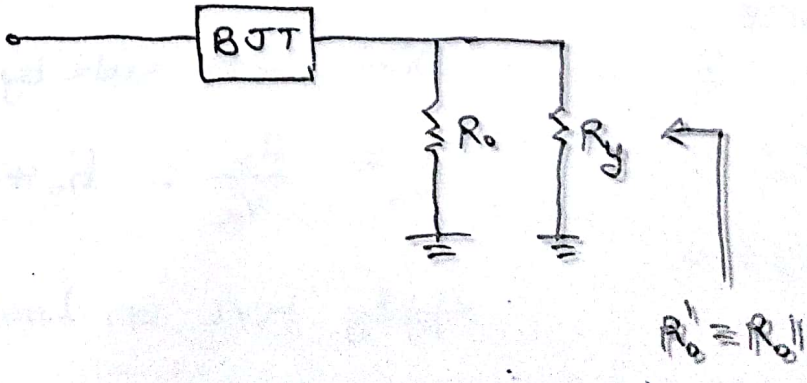
$$\frac{1}{R_o} = \frac{I_x}{V_x} = h_o - \frac{h_f h_{rf}}{R_s' + h_i}$$

Input Res. : R_i'



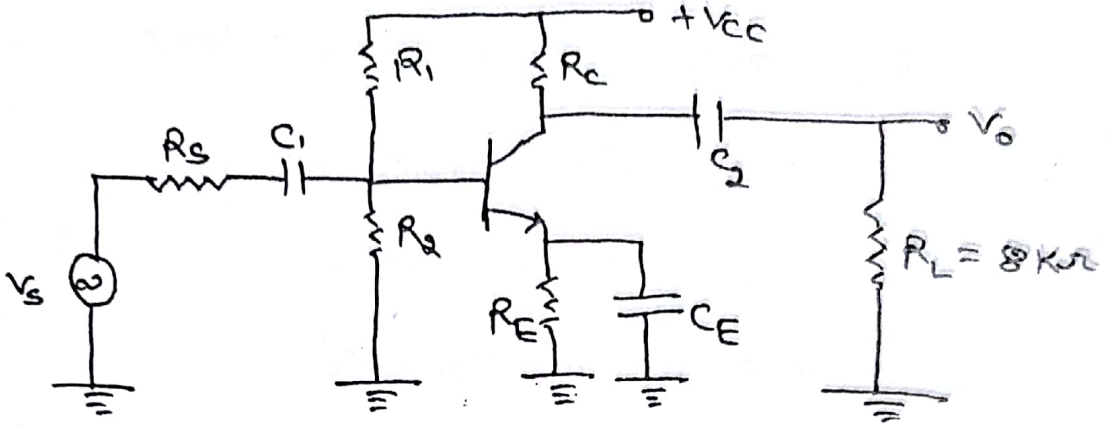
$$R_i' = R_x \parallel R_i$$

output Resistance:



ample: In the Amplifier shown BJT has $h_{fe} = 60$, $h_{re} = 2 \times 10^{-4}$ and $h_{oe} = 25\ \mu\mho$. Calculate voltage gain, input Resistance, output Resistance, current Gain. Draw the AC equivalent ckt. also.

Lution:



Given $R_1 = 80K\Omega$, $R_2 = 20K\Omega$, $R_c = 5K\Omega$, $R_L = 8K\Omega$

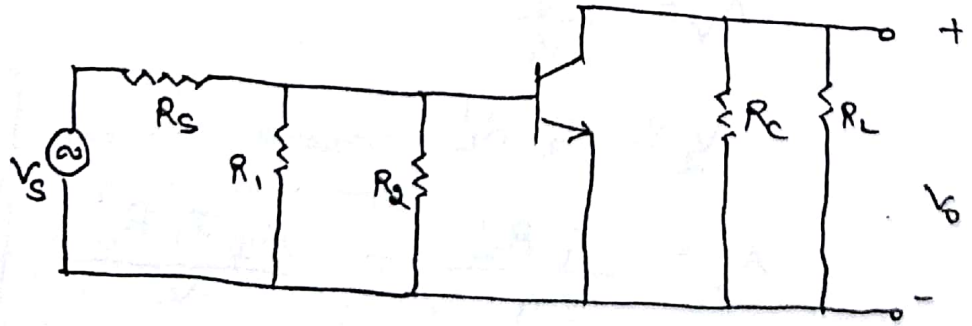
nalysis: Given circuit is common emitter Amplifier (VDB).

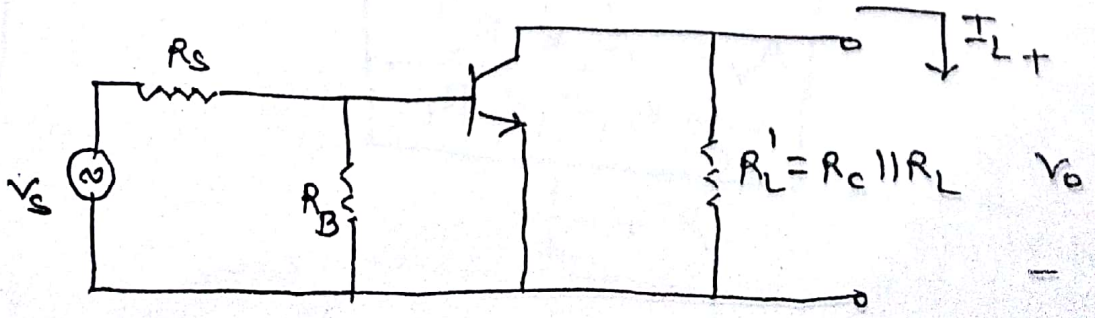
tep 1. Draw the AC equivalent circuit of the CE Amp.

→ By Short ckt. all the capacitor.

→ By Ground the DC voltage source.

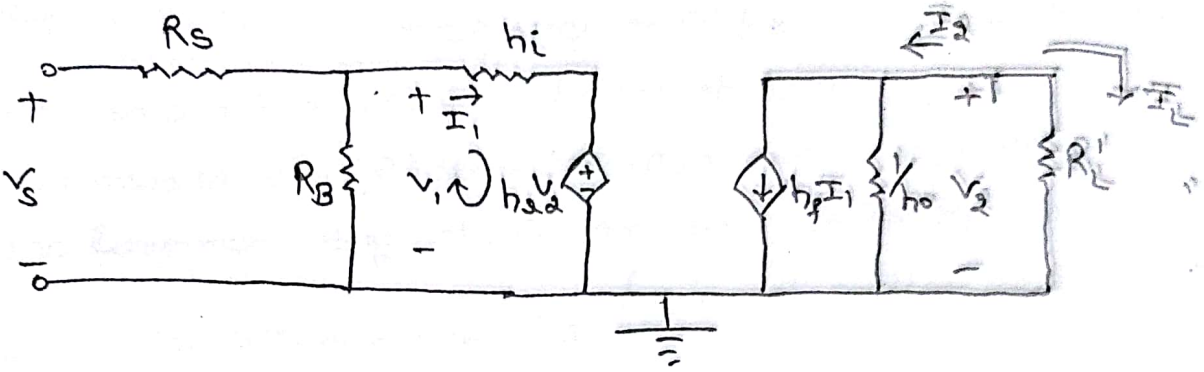
→ Replace the transistor with their eq. model (h-parameter model).





1. $R_B = R_1 \| R_2 = 80 \| 20 = \frac{80*20}{80+20} = 16\,K\Omega$

2. $R_L' = R_C \| R_L = \frac{5*8}{5+8} = \frac{40}{13} = 3.07\,K\Omega$



1. Current Gain: $\longrightarrow$ $A_I = \frac{I_L}{I_1}$

By Current Divison Rule

$$I_L = \frac{-h_f I_1 * 1/h_o}{1/h_o + R_L'} = \frac{-h_f I_1}{1+h_o R_L'}$$

$$A_I = \frac{I_L}{I_1} = \frac{-h_f}{1+h_o R_L'} = \frac{-60}{1+(25*10^{-6})(3.07*10^3)}$$

$$\boxed{A_I = -55.72}$$

2. Input Resistance: $\longrightarrow$ $R_i = \frac{V_1}{I_1}$

KVL in Input Loop.

$$+V_1 - h_i I_1 - h_r V_2 = 0$$

$$V_1 = h_i I_1 + h_r (I_L R_L')$$

$$V_1 = h_i I_1 + h_r A_I I_1 R_L'$$

$$V_1 = I_1 (h_i + h_r A_I R_L')$$

$$R_i = \frac{V_1}{I_1} = h_i + h_r A_I R_L'$$

$\because V_2 = V_L = I$

$\because A_I = \frac{I_L}{I_1}$

$I_L = A_I$

$$R_i = 1.5\,K\Omega + 2.5 * 10^{-4}\,(-55.72)\,(3.07K\Omega)$$

$$R_i = 1.465\,K\Omega$$

But As you know

$$R_i' = R_i \,||\, R_B$$

$$= 1.465 \,||\, 16$$

$$\boxed{R_i' = 1.34K\Omega}$$

Voltage Gain: $A_v = \frac{V_o}{V_i}$

From Analysis

$$A_v = A_I * \frac{R_L'}{R_i}$$

$$= -\frac{55.7 * 3.07}{1.465}$$

$$\boxed{A_v = -116.72}$$

Output Resistance: R_o

$$\frac{1}{R_o} = h_o - \frac{h_f h_r}{R_s' + h_{ie}}$$

$$= 25*10^{-6} - \frac{60 * 2*10^{-4}}{0.94*10^3 + 1.5*10^3}$$

$$R_o = 49.8K\Omega$$

As you know

$$o' - R_o \,||\, R_L = 49.8 \,||\, 5 = 4.5K\Omega$$

↓
Junction field effect Transistor (JFET)

↓
Metal oxide Field effect Transistor (MOSFET) (or) Insulated gate FET (IGFET)

Junction field Effect Transistor (JFET):

The JFET are further classified as:

1. N- channel JFET.
2. P- channel JFET.

N-channel JFET: 1. Construction:

In N- channel JFET an N-type Si bar, referred to as channel, has two smaller piece of P-type Si material diffused on the opposite sides of its middle part, forming P-N junction.

The two P-N junction forming diodes (or) gates are connected internally and common terminal called the gate terminal is brought out.

ohmic contacts (direct electrical connection) are made of two ends of channel, one lead called Source terminal 'S' and the other terminal is drain terminal 'D'.

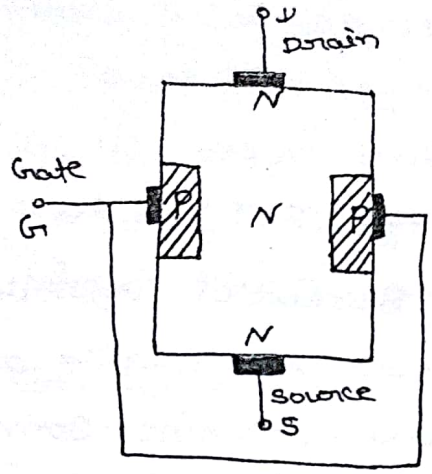


Fig 1(a)

N-channel JFET

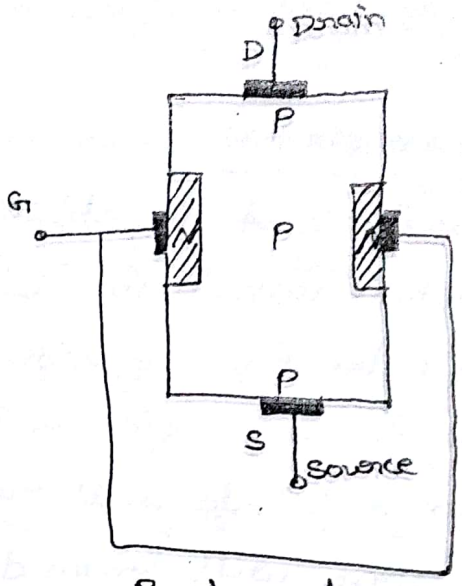
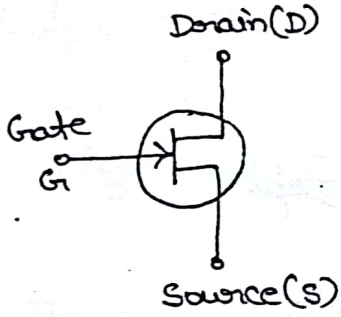
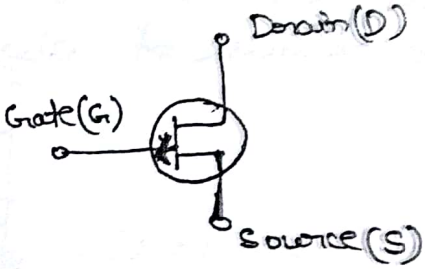


Fig 1(b)

P-channel JFET



n-channel JFET



P-channel JFET

al working of JFET: (N-channel)

In JFET, the P-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reversed biased ~~conditions. Since the current in a~~ P-n junction is extremely small

We consider three cases for understanding working of JFET:

1. No Bias condition
2. $V_{GS} = 0$ and V_{DS} = Some Positive value.
3. $V_{GS} < 0$ and V_{DS} = Some Positive value.

used as an amplifier. V_p is the minimum voltage.

3. Breakdown Region:

In this region, drain current increases rapidly as the drain to source voltage is increased. It is because of the breakdown of gate source junction due to Avalanche effect.

Transconductance curve (or) Transfer characteristics:

The curve between drain current and gate source voltage (V_{GS}) of JFET at constant drain source voltage is known as transfer characteristics.

The Relationship between I_D and V_{GS} is defined by Shockley's equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

The Squared term of the equation will result in non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

The transfer curve can be obtained by using shockley equation (or) from output characteristics.

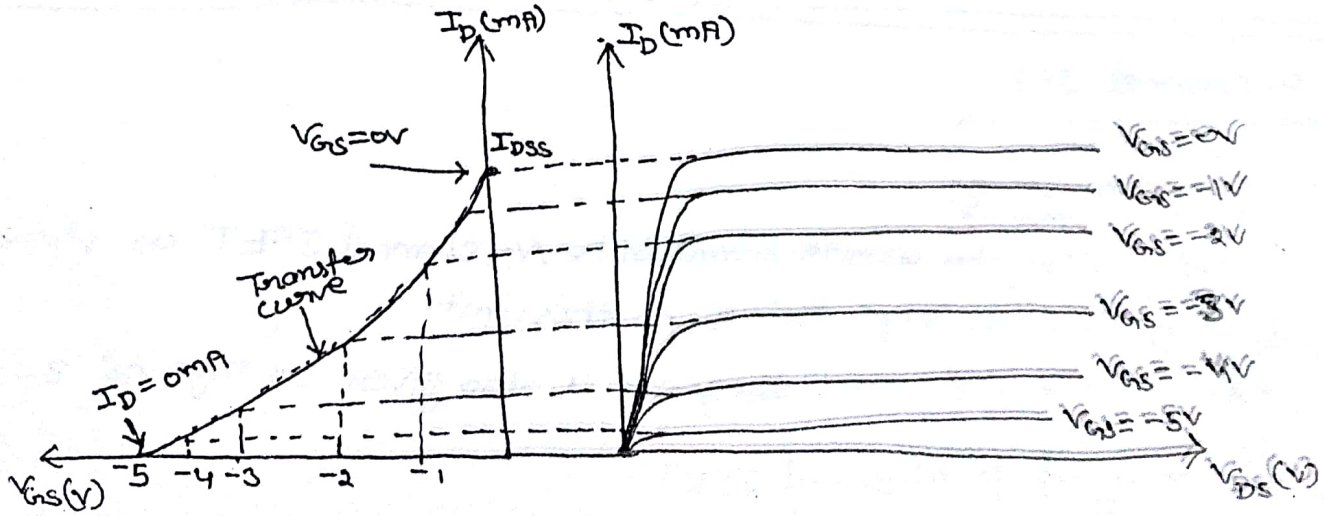


Fig: Transconductance (or) Transfer curve.

The level of V_p and I_{DSS} define the limits of the transfer curve on both axes.

from Shockley equation:

when $V_{GS} = 0V$

$$I_D = I_{DSS}\left[1 - \frac{0}{V_P}\right]^2$$

$$I_D = I_{DSS}$$

when $V_{GS} = 0.3\,V_P$

$$I_D = \frac{I_{DSS}}{2}$$

when $V_{GS} = 0.5V$

$$I_D = I_{DSS}\left[1 - \frac{0.5V_P}{V_P}\right]^2$$

$$I_D = \frac{I_{DSS}}{4}$$

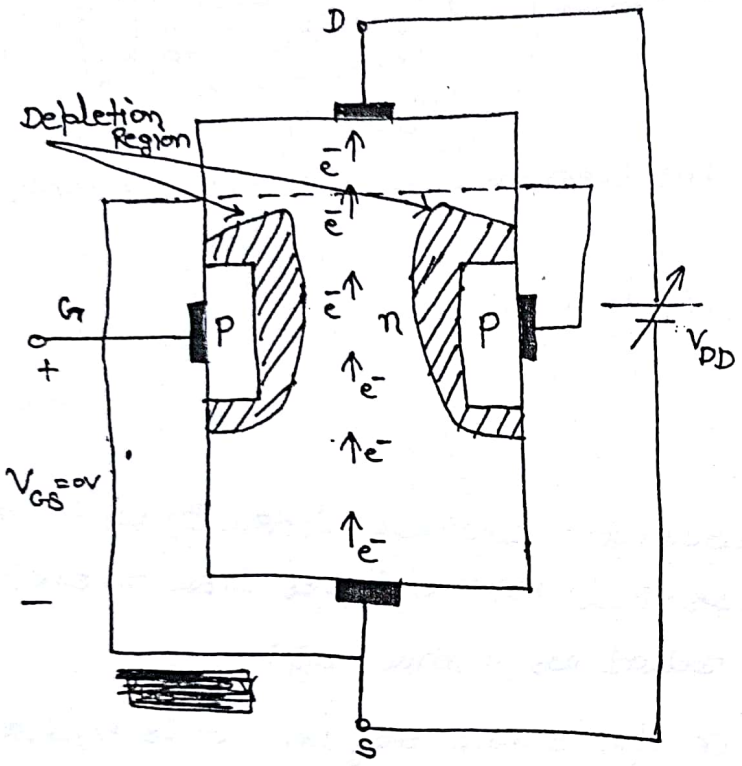
when $V_{GS} = V_P$

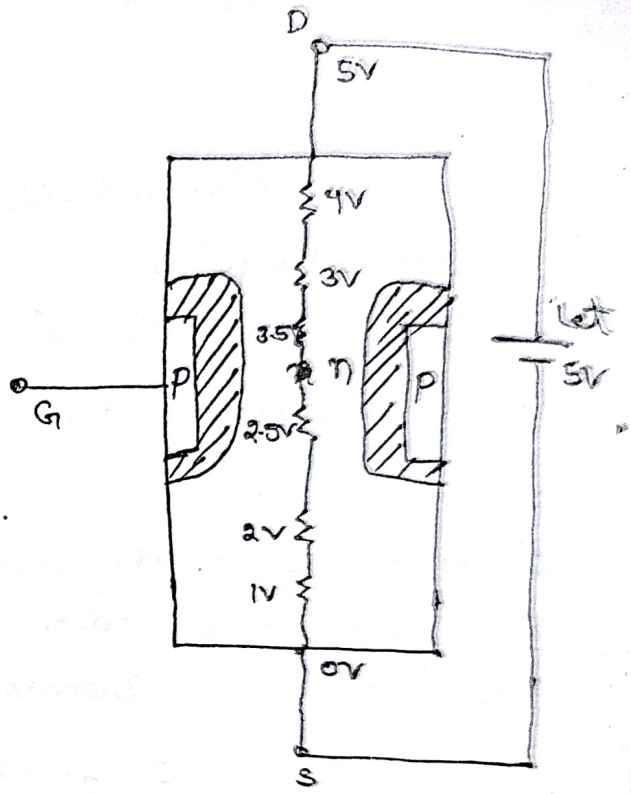
$$I_D = 0\ mA$$

By these values we can also draw the transfer curve-

2. The widening of depletion region towards drain side compared to towards source side as effect of positive potential of V_{DS} is more towards drain which causes reverse bias in P-n junction as

$$V \propto \frac{1}{d} \qquad d = \text{distance.}$$





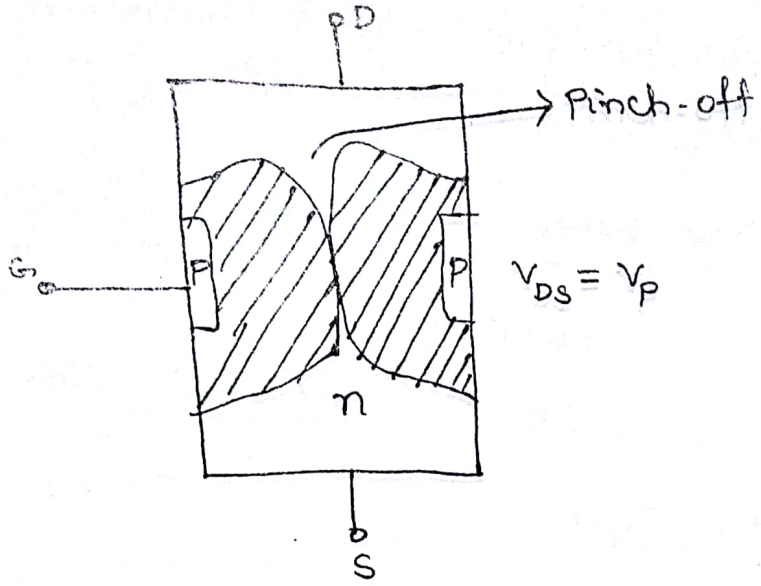
Path of charge flow clearly indicates that drain and source currents are equivalent-

$$I_D = I_S.$$

Flow of charge is relatively limited solely by resistance of n- channel between drain and source.

If V_{DS} increased then I_D also increases, But if V_{DS} is increased to a high level up to V_p then depletion region will widen causing a noticable reduction in the channel width.

So, if $V_{DS} = V_p$, then because of very high reverse bias depletion region of drain terminal, the two depletion region will ~~touch~~ touch each



The value of V_{DS} (i.e V_p) at which this condition (Pinch-off) occur, is known as Pinch-off voltage.

The term Pinch-off suggest that the current I_D is Pinched-off and drops to 0A.

But actually this does not happens, At pinch-off voltage (V_p), Drain current (I_D) maintain a Saturation level (I_{DSS}) with current of very high density.

This can be verified by the following fact:

The absence of depletion drain current would remove the possibility of different potential levels through the n-channel material to establish varying levels of reverse bias along p-n junction.

As V_{DS} is increased beyond V_p, the region of close encounter between the two depletion region will increase in length along channel, but the level of I_D remains essentially the same.

If $V_{DS} > |V_p|$ then $I_D = I_{DSS}$

1. Under No-Bias condition.

   * Try to write in similar way to N-channel JFET.

2. $V_{GS} = 0V$ and V_{DS} = Some Negative value.

   * Try to write in similar way, but V_{DS} is negative here.

3. $V_{GS} > 0V$ and V_{DS} = Some negative value.

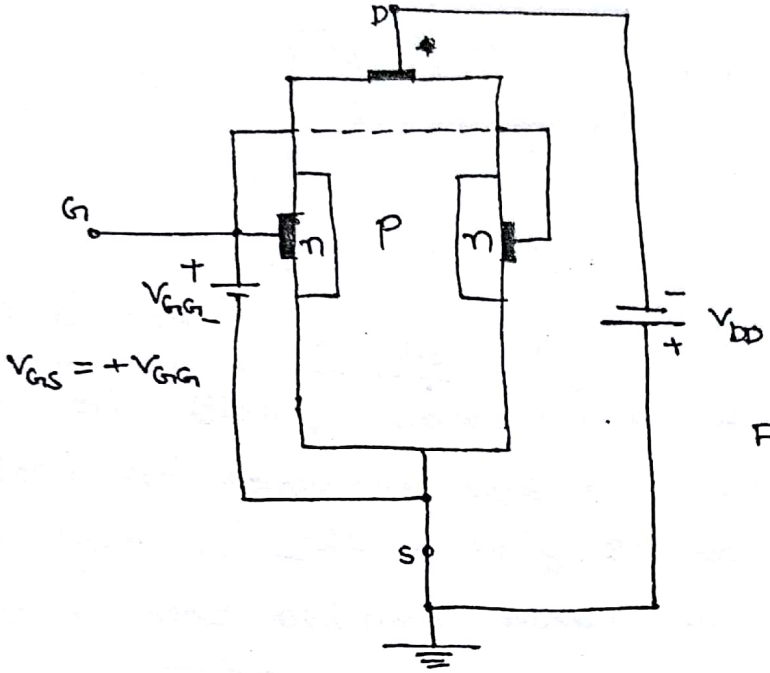


Fig- P-channel JFET-

   * Try to write working here.

etal oxide semiconductor Field Effect Transistor: MOSFET of

(or)

insulated Gate Field Effect Transistor (or) IGFET :

MOSFET

on the Basis of construction

↓ Depletion Type

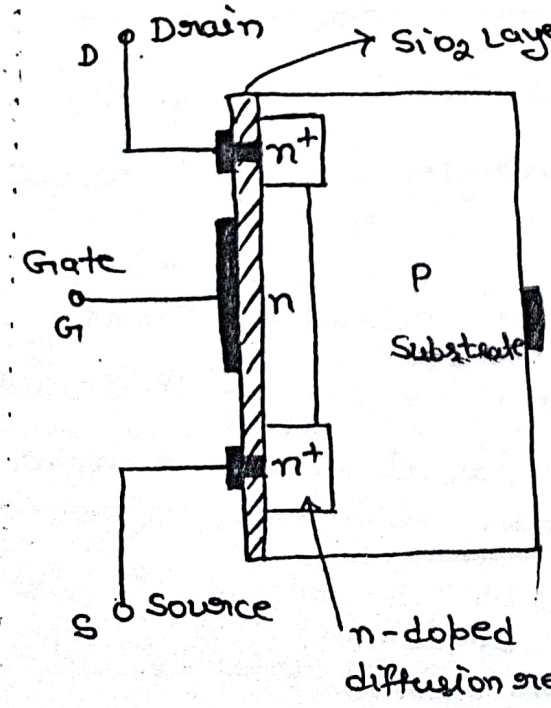
↓ Enhancement Type

pletion Type MOSFET: (n-channel)

Its operation is similar to JFET between cut-off and saturation at I_{DSS}, but it also have added features of characteristics that extended into region of opposite polarity for V_{GS}.

sic construction:

ion n-channel a slab of P-type is formed from silicon ase and is known as Substrate.



⇒ n-channel Depletion Type MOSFET

the
circuit.

it is foundation upon which device will be constructed. N-type region is formed through diffusion after that SiO_2 layer is

formed.

Source and Drain terminal are connected through metallic contact to n-doped region, linked by an n-channel.

Gate is also connected to a metal contact surface but remains insulated from the n-channel by very thin SiO_2 layer.

Thus SiO_2 layer provides insulation between gate terminal and channel. It means there is no electri Connection between gate and channel. So, it is also called insulated Gate FET (IGFET).

Because of SiO_2 layer MOSFET have very High Impedance as compared to JFET. It also support fact that gate current (I_G) is zero for dc bi configurations.

Basic operation and characteristics:

For understanding the working of MOSFET. It have mainly 3 classification for n-channel.

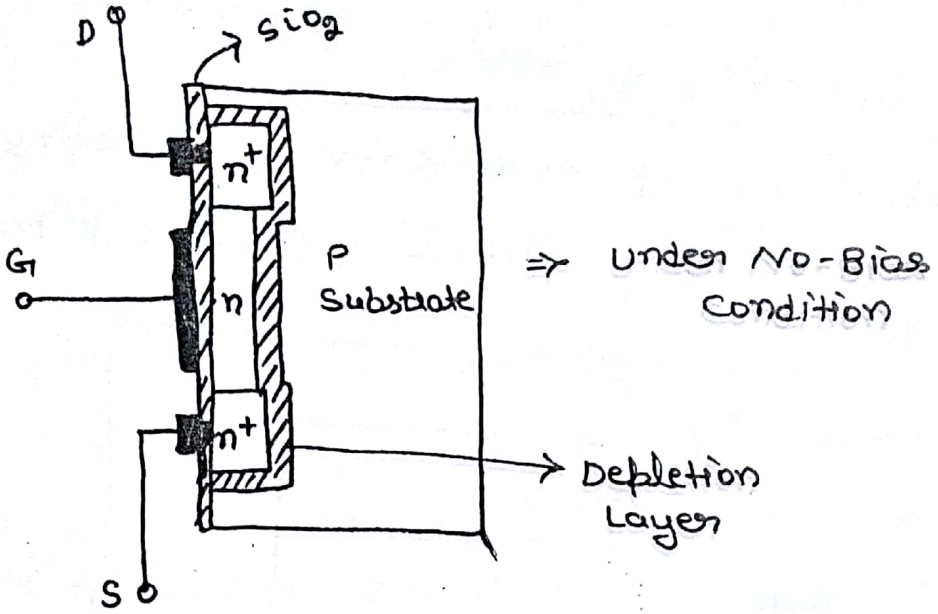
1. No Bias
2. when $V_{GS} = 0V$, $V_{DS} > 0V$ (some Positive value)
3. when $V_{GS} < 0V$ (negative), $V_{DS} > 0V$ (some Positive value)

Depletion Mode.

If we make $V_{GS} > 0V$, $V_{DS} > 0V$ ⇒ Enhancement mode.

1. No-Bias:

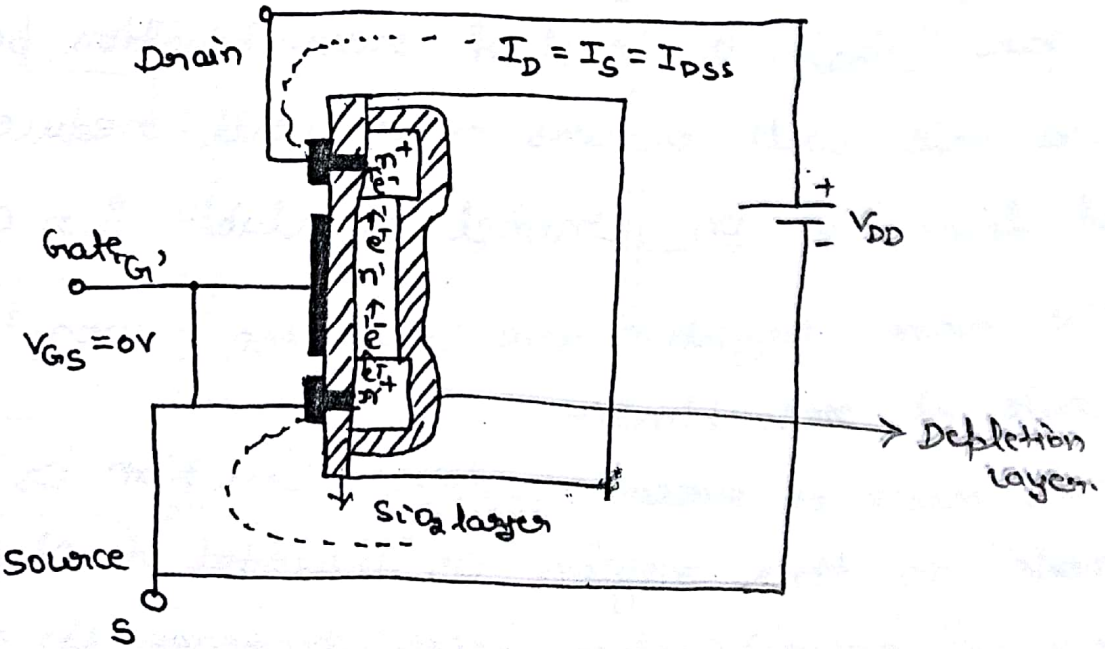
At no bias depletion region will be formed between n and P Substrate.



When $V_{GS} = 0V$ and $V_{DS} > 0V$

Under this Biasing condition e^- from n-channel will ...ute be attracted towards positive potential of drain and ...t source terminal will supply electrons. So, closed path ...bias will be formed between source and drain.

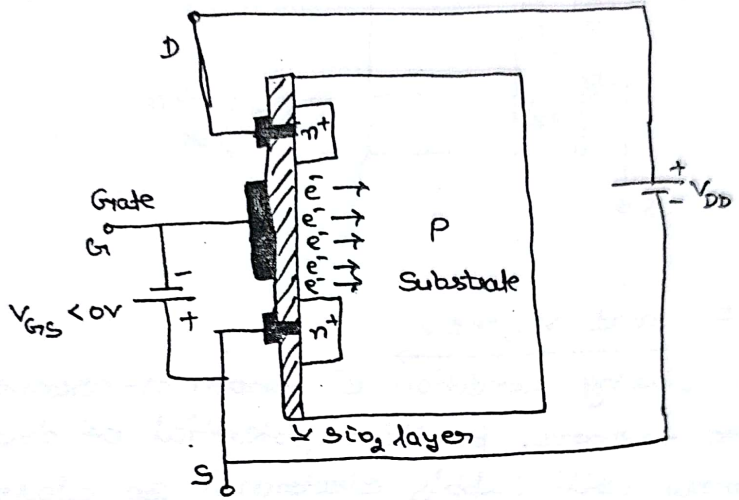
$$I_D = I_S = I_{DSS}$$



...t the same time depletion layer will also become wide ...due to application of V_{DS}. But this can not affect the ... flow of majority charge carrier through channel.

3. when V_{GS} = -ve , V_{DS} > 0V :

Due to application of negative (-ve) gate voltage it will repel electron of n-channel and attract hole from p-substrate.



During this process some of e^- and hole will recombine. Depending on the magnitude of negative bias established by gate (V_{GS}), a level of recombination between e^- and hole will occurs that will reduce the no of free e^- in channel available for conduction.

The more negative the bias, the higher the rate of recombination.

This mode of ~~recombination~~ operation is called depl mode as this region is depleted of charge carrie due to recombination with increase in negative V_{GS}

When $V_{GS} > 0V$, $V_{DS} > 0V$:

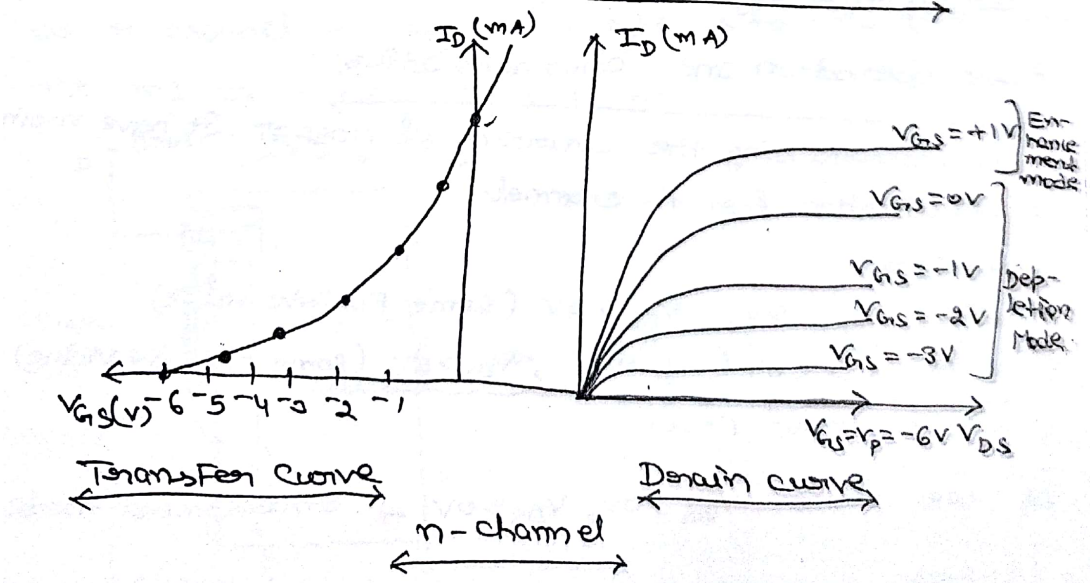
For Positive value of V_{GS}, Positive gate will draw additional Free electrons from the P-type Substrate, and establish new carrier.

As we increase $+V_{GS}$, I_D will also increase. It means it is enhancing the level of free carriers in the channel. This mode of operation is called enhancement region.

Depletion type MOSFET follow shockley eqn:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

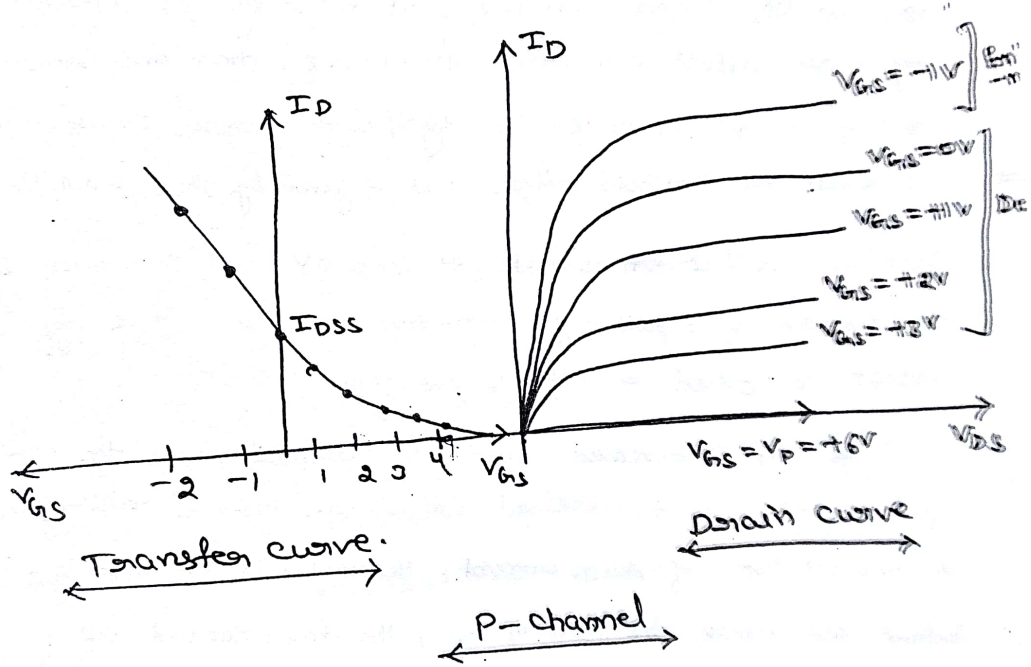
Transfer curve and Drain curve for n-channel Depletion type MOSFET :



Characteristics of P-channel Depletion Type MOSFET:

For P-channel

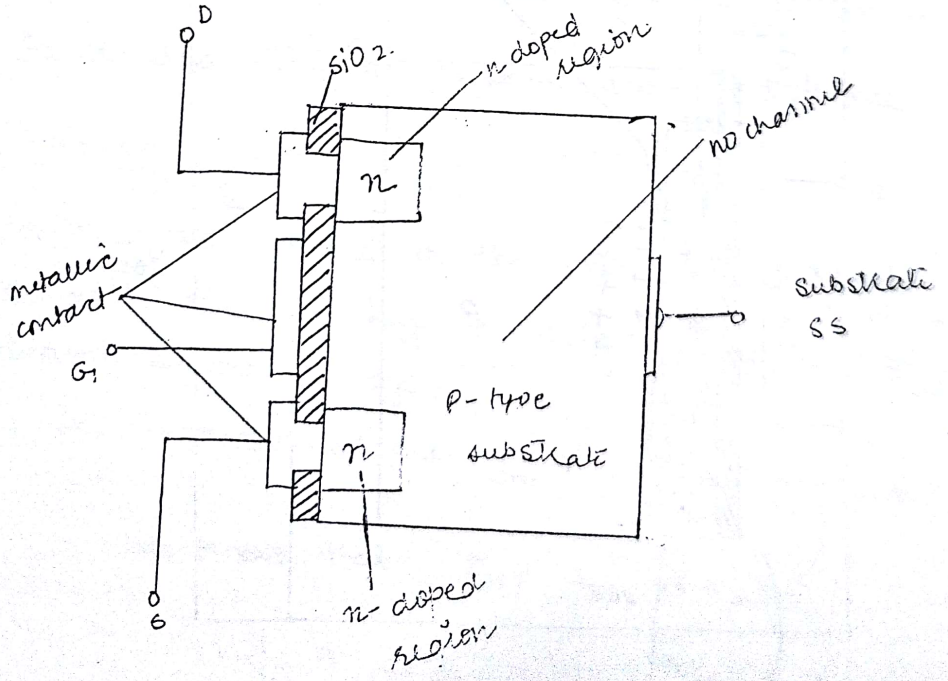
1. $V_{GS} = 0V$, $V_{DS} < 0V$
2. $V_{GS} > 0V$, $V_{DS} < 0V$
3. $V_{GS} < 0V$, $V_{DS} < 0V$



Enhancement-Type MOSFET

Basic Construction :

The basic construction of the n-channel enhancement-type MOSFET is shown in figure below. A slab of p-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to n-doped regions. The construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.



JFET Parameters:

JFET has certain parameters which determines the performance. Such parameters are:

1. AC drain Resistance.
(ii) Transconductance
(iii) Amplification factor
(iv) DC Drain Resistance

AC Drain Resistance: (r_d)

It is defined as the ratio of change in drain-Source voltage (V_{DS}) to change in drain current at Constant gate-Source voltage and is denoted by r_d.

$$\text{AC drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at Constant } V_{GS}$$

It is also called the dynamic drain resistance.

Transconductance: (g_m)

It may be defined as the ratio of change in drain current to the change in gate-Source voltage at Const drain-Source voltage.

ie Transconductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ at Constant V_{DS}

we know that $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$g_m = \frac{\Delta I_D}{}$

$$g_m = -\frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Substituting $V_{GS} = 0$

$$g_{m_0} = -\frac{2I_{DSS}}{V_P}$$

$$g_m = g_{m_0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Amplification Factor:

It is defined as the ratio of change in drain-source voltage to the change in gate-source voltage at constant drain current, and is denoted by μ.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D.$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_d \times g_m$$

μ = AC drain resistance × transconductance

DC Drain Resistance: (R_{DS}) It is also called the static (or) ohmic resistance of the channel and is defined as ratio of drain source voltage and drain current.

i.e $$R_{DS} = \frac{V_{DS}}{I_D}$$

Example: when a reverse Bias voltage of 10V is applied between gate and source of JFET, the gate current is 0.001 μA. Determine resistance between gate and source.

Solution:

$$V_{GS} = 10\,V$$

$$I_G = 0.001\,\mu A = 1 \times 10^{-9}\,A$$

$$R_{GS} = \frac{V_{GS}}{I_G} = \frac{10}{1 * 10^{-9}} = 10{,}000\,M\Omega.$$

Example: when Drain source voltage is changed by 1.5 volts, the change in drain current is of 120 μA, the gate-Source voltage remaining uncharged. Determine the ac drain resistance?

Solution:

$$\Delta V_{DS} = 1.5V$$

$$\Delta I_D = 120 * 10^{-6}\,A$$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1.5}{120 * 10^{-6}} = 12.5\,K\Omega.$$

Example: A JFET has $V_p = -4.5\,V$, $I_{DSS} = 10\,mA$, and $I_D = 2.5\,mA$ Determine the transconductance.

Solution:

$$I_{DSS} = 10\,mA$$

$$V_p = -4.5\,V$$

$$I_D = 2.5\,mA$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \Rightarrow V_{GS} = V_p\left[1 - \sqrt{\frac{I_D}{I_{DSS}}}\right]$$

$$= -2.25V$$

$$g_m = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right] = \frac{-2 \times 10 \times 10^{-3}}{-4.5}\left[1 - \frac{-2.25}{-4.5}\right]$$

FET Biasing:

For FET Biasing i.e DC analysis we need biasing circuit for maintaining stability of Q-point.

for D.C equivalent circuit: 1. ground ac source.

2. open circuit all capacitor.

3. $I_G \cong 0A$ so that $V_{R_G} = I_G R_G = 0V$

The zero volt drop across R_G permits replacing R_G by short circuit.

1. Fixed Bias configuration:

The simplest of biasing arrangements for the n-channel JFET, referred to as the fixed bias configuration is shown in figure:

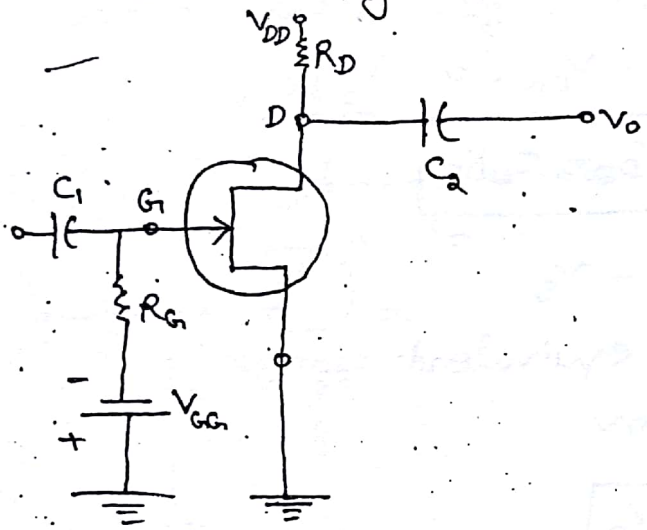


Fig: Fixed Bias configuration.

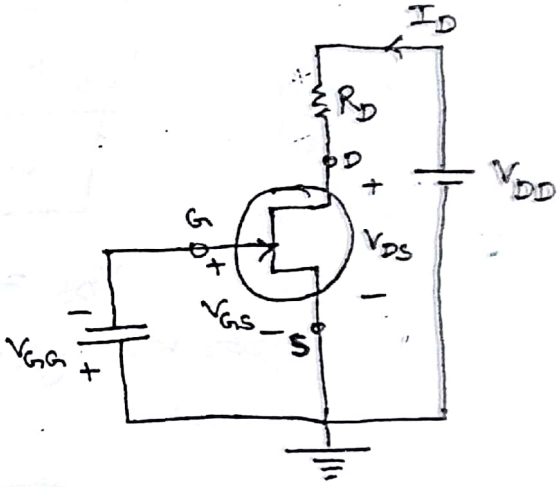


Fig: DC equivalent circuit.

As shown in fig:, for DC analysis all the coupling capacitor are open circuit.

The negative terminal of the battery is connected directly to the defined positive potential of V_{GS}, which clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}.

By Applying KVL

$$-V_{GG} - V_{GS} = 0$$

As we know, from Schokley's equation

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Put $V_{GS} = -V_{GG}$

$$I_D = I_{DSS}\left[1 - \frac{(-V_{GG})}{V_P}\right]^2$$

$$I_{D(on)} = I_{DQ}$$

By applying KVL at output side.

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = V_D - V_S$$

for the given DC equivalent circuit

$$V_S = 0V$$

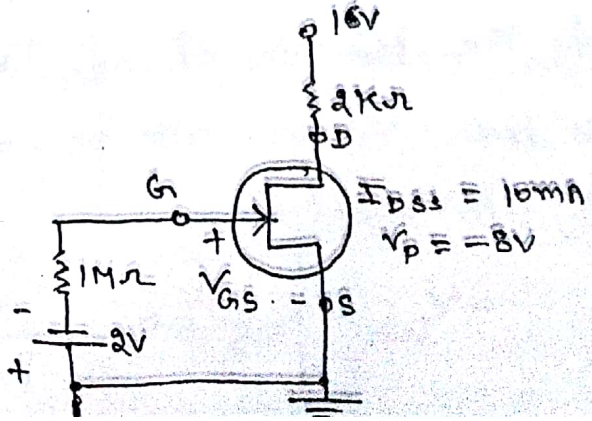
So that, $V_{DS} = V_D$

Similarly, $V_{GS} = V_G - V_S$ $\quad \because V_S = 0$

$$V_{GS} = V_G$$

Example:1) Determine the following for the network:

(i) V_{GSQ} (ii) I_{DQ} (iii) V_{DS} (iv) V_D (v) V_G (vi) V_S



Solution: (i) $V_{GSQ} = -V_{GG}$

$= -2V$

(ii) I_D (or) $I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$= 10mA\left[1 - \frac{-2}{-8}\right]^2 = 10\left[1 - \frac{1}{4}\right]^2 = 5.625mA$

(iii) $V_{DS} = V_{DD} - I_D R_D \Rightarrow 16V - (5.625mA) * (2K\Omega)$

$= 16V - 11.25V = 4.75V$

(iv) $V_D = V_{DS} = 4.75V$

(v) $V_G = V_{GS} = -2V$

(vi) $V_S = 0V$

~~2. Self Bias configuration:~~ 2. By Graphical Analysis

1. Apply KVL at I/P side to find V_{GS}

$$\boxed{V_{GS} = -V_{GG}}$$

2. By putting value of V_{GS} in shokley equation find I_D

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

From these four value plot the transfer curve.

3. Intersection point of transfer curve and V_{GS} curve of step 1 will give Q-point (I_{DQ}, V_{GSQ})

4. Applying KVL at o/p side

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

$V_S = 0$

$V_D = V_{DS}$

$V_G = V_{GS}$

These four steps are used for graphical analysis of any Biasing circuit.

Graphical Analysis of Example(1):

1. By KVL at I/P side

$$-2 - V_{GS} = 0$$

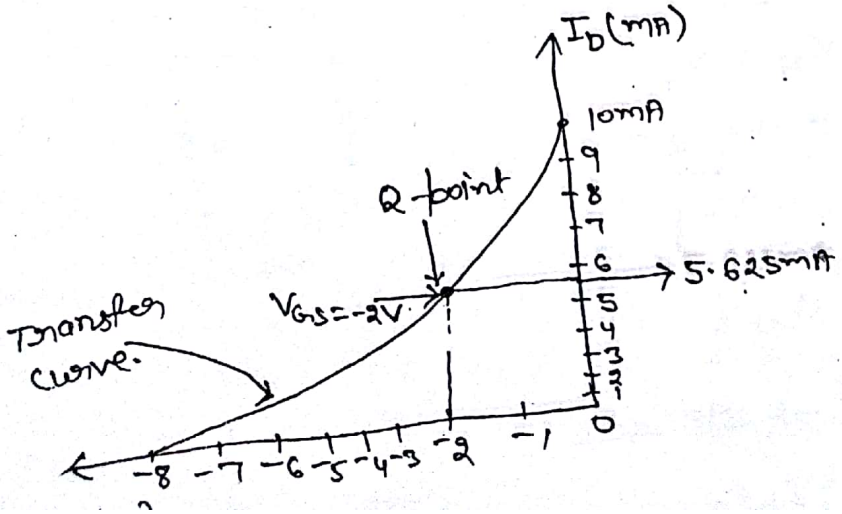
$$V_{GS} = -2V \quad (or)\ V_{GSQ} = -2V$$

2. Plot transfer curve.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

V_{GS}	I_D
0	10mA
$0.3V_P$	5 mA
$0.5V_P$	2.5 mA
V_P	0 mA

$$I_{DQ} = 10mA\left[1 - \frac{-2}{-8}\right]^2 = 5.625mA$$



$$V_{DS} = V_{DD} - I_D R_D$$

$$\Rightarrow 16 - 5.6 * 2 = 4.8V$$

$$V_G = V_{GS} = -2V$$

$$V_D = V_{DS} = 4.8V$$

$$V_S = 0V$$

2. Self-Bias configuration:

The Self-Bias configuration eliminates the need for two dc supplies. The controlling gate-to source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in fig.

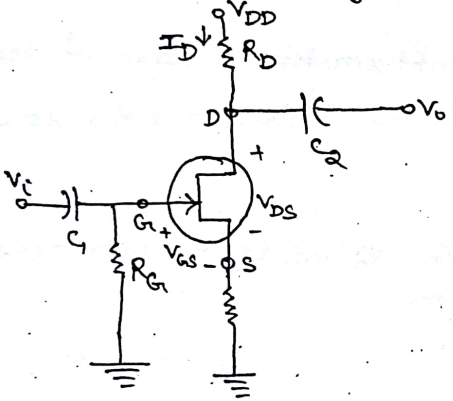


Fig: JFET Self-Bias configuration

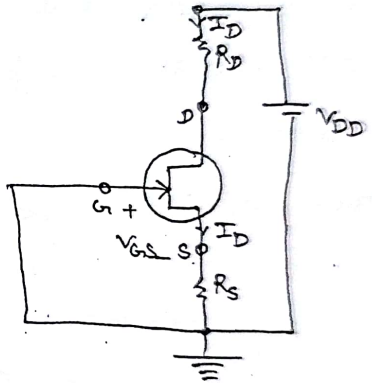


fig: DC equivalent circuit.

KVL at I/P side

$$-V_{GS} - I_D R_S = 0$$

$$\boxed{V_{GS} = -I_D R_S}$$

Find I_D By putting V_{GS} in Shockley's equation.

By applying KVL at o/p side

$$-V_{DS} - I_D R_D - V_{DD} - I_D R_S + V_{DD} = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

$$V_S = I_D R_S$$

$$V_{GS} = V_G - V_S$$

$$V_G = 0$$

$$V_{GS} = V_S$$

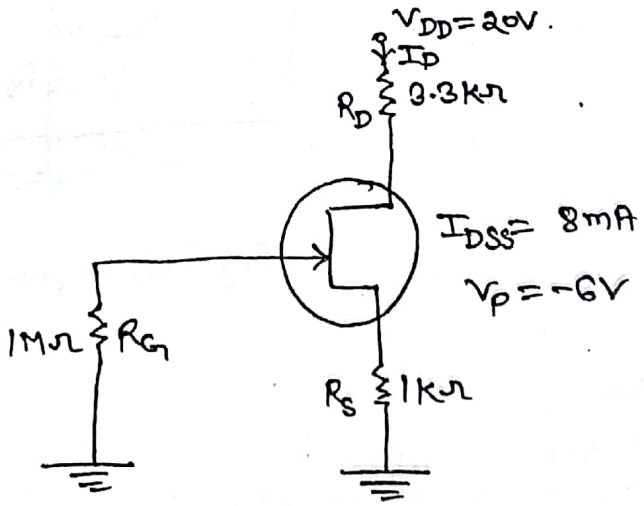
$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S = V_{DD} - \underbrace{I_D R_D}_{V_{RD}} - I_D R_S + I_D R_S$$

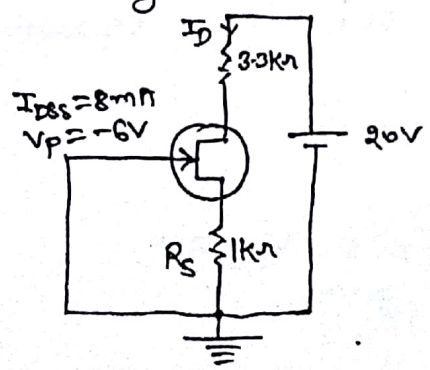
$$V_D = V_{DD} - V_{RD}$$

This is called Self-Bias configuration, because of feedback (I/P) voltage is provided as Input due to source voltage.

Example: Find V_{GSQ}, I_{DQ}, V_{DS}, V_S, V_D and V_G for given network



Solution: By Mathematical approach



By applying KVL at I/P side

$$-V_{GS} - I_D R_S = 0$$

$$V_{GS} = -I_D R_S$$

$$V_{GS} = -I_D (1k\Omega)$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = 8mA\left[1 - \frac{-I_D}{-6}\right]^2$$

$$I_D = 8 + \frac{I_D^2}{9} - \frac{8}{3}I_D$$

$$9I_D = 72 + I_D^2 - 24I_D$$

$$I_D^2 - 33I_D - 72 = 0$$

$$I_D = \frac{+33 \pm \sqrt{33^2 + 4*1*72}}{2}$$

$\boxed{I_{DQ} = 2.3mA}$ choose such value of I_D for which V_{GS} = -ve (n-channel)

So that $\boxed{V_{GS} = -2.3\ V}$

By applying KVL at output side

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$= 20 - 2.3\ (3.3 + 1)$$

$\boxed{V_{DS} = 10.11V}$

$\boxed{V_{GS} = -2.3V}$

$\boxed{V_S = I_D R_S = 2.3 * 1 = 2.3V}$

$\boxed{V_G = 0V}$

$$V_D = V_{DS} + V_S$$

$$= 10.11 + 2.3$$

$\boxed{V_D = 12.41V}$

⇒ By Graphical Analysis

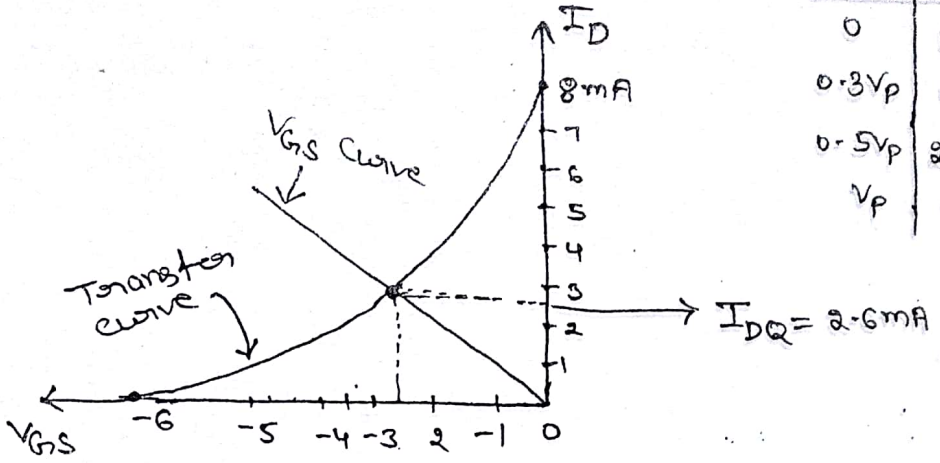
By applying KVL at I/P side

$$V_{GS} = -I_D R_S$$

$$\therefore V_{GS} = -I_D(1K\Omega)$$

Plot transfer curve

V_{GS}	I_D
0	8 mA
$0.3V_p$	4 mA
$0.5V_p$	2 mA
V_p	0 mA



$$V_{GS} = -2.6V$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \Rightarrow 20 - 2.6(1+3.3) = 8.82V$$

$$V_{DS} = 8.82V$$

$$V_S = I_D R_S \Rightarrow 2.6V$$

$$V_G = 0$$

$$V_D = V_{DS} + V_S = 8.82 + 2.6 = 11.42V$$

(or)

$$V_D = V_{DD} - I_D R_D = 20 - 2.6 * 3.3 = 11.42V$$

3. Voltage-Divider Biasing | Potential Divider Biasing :

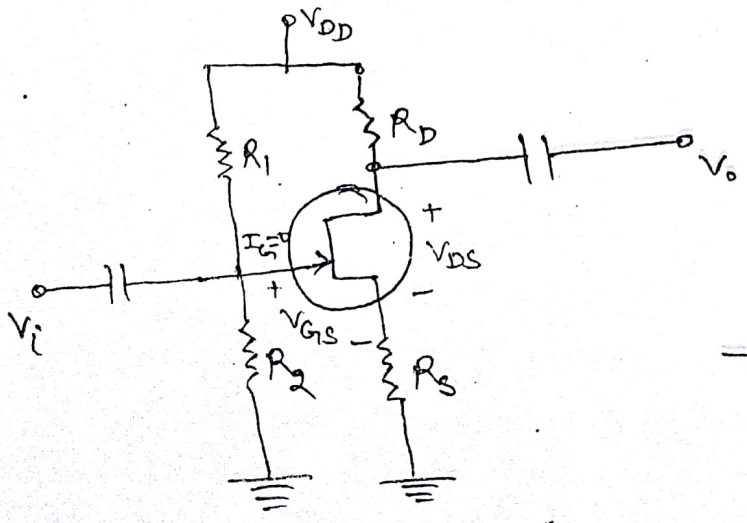


Fig: voltage-Divider Bias ckt

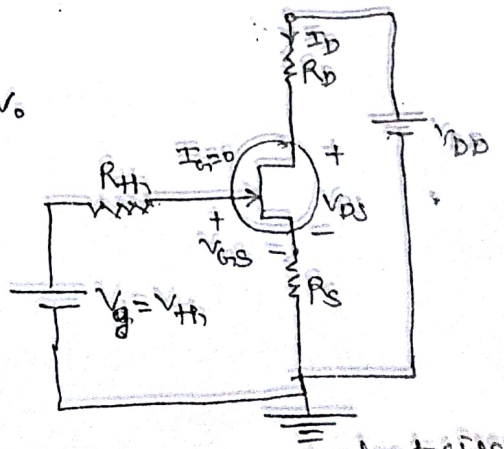


Fig: DC equivalent circuit

$$V_G = V_{th} = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{Rth} = I_g R_{th} = 0V \quad \text{as } I_G = 0mA$$

we solve this biasing circuit only by graphical approach.

$$V_g - V_{GS} - I_D R_S = 0$$

$$\boxed{V_{GS} = V_g - I_D R_S}$$

Plot V_{GS} curve for different value of I_D like as

$$V_{GS} = V_g \quad \text{for } I_D = 0$$

$$I_D = \frac{V_g}{R_S} \Big|_{V_{GS} = 0V}$$

Increasing the value of R_S result in lower Quiscent value of I_D and more negative value of V_{GS}.

* Plot transfer curve using schokley equation.
* Intersection of V_{GS} curve and transfer curve gives Q-point. (I_{DQ}, V_{GSQ}).
* Applying KVL at o/p side

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$\boxed{I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}}$$