

END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER 2015

Paper Code: BCA-203

Subject: Computer Architecture
(Batch 2011 Onwards)

Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions including Q.no.1 which is compulsory.
Select one question from each unit.

Q1 Attempt the following (any ten): (10x2.5=25)

- (a) Give difference between RISC and CISC.
- (b) List various Logic Microoperations.
- (c) Explain Instruction formats, describe its various parts.
- (d) A 8 bit register contain the binary value 10011100. What is the register value after an arithmetic shift right? Determine the register value after logic shift left.
- (e) Explain the importance of memory hierarchy in computer system.
- (f) Draw diagram showing arithmetic pipeline for floating point addition and subtraction.
- (g) Explain Register Transfer Language.
- (h) Draw 4-bit combinational circuit decremter.
- (i) For a given below 16 bit instruction, give the equivalent four digit hexadecimal code and explain what is the that instruction.
- (j) Explain locality of reference in context with cache memory.
- (k) A bus organized CPU has 16 register with 32 bits in each, an ALU and a destination decoder.
 - (i) How many multiplexer are there in A bus and what is the size of each multiplexer?
 - (ii) How many selection inputs are needed for MUX A and MUX B?
- (l) Convert the following arithmetic expression from infix to reverse polish notation.
 $A * B + (C/D + E * F)$.

Unit-I

- Q2 (a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operation in conjunction with the input carry C_{in} . Draw the logic diagram for the first two stages. (6.5)

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A+B$ (add)	$D = A+1$ (increment)
1	$D = A-1$ (decrement)	$D = A+B'+1$ (subtract)

- (b) Design and describe Control unit of basic computer. (6)
- Q3 (a) Draw adder and subtractor and explain its logic circuit. (6.5)
(b) By using flowchart explain its various phases of an instruction cycle and interrupt cycle? (6)

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BCA-203

Unit-II

- Q4 (a) Explain various Addressing Modes used in Instruction format. Give numerical example to explain. (6.5)
- (b) Write a program to evaluate the arithmetic statement with zero, one, two and three address instruction. (6)

$$X = \frac{A-B+C}{G+H*K}$$

- Q5 (a) What is Pipelining? Explain Instruction Pipelining, and three major difficulties that cause instruction pipeline to deviate from its normal operation. (6.5)
- (b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in six-segment pipeline with clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved? (6)

Unit-III

- Q6 (a) Explain functioning of Booths Algorithm and Multiply (+15) x (-13) using general multiplication algorithm of Booth algorithm. (6.5)
- (b) Explain the DMA control with the help of block diagram. (6)
- Q7 (a) Explain the difference between the daisy chaining priority and parallel priority interrupts. Draw the diagram to explain their working. (6.5)
- (b) Divide using division algorithm 10100011 by 1011. (6)

Unit-IV

- Q8 (a) Using Block diagram explain the logic used in the associative memory. (6.5)
- (b) How many 128x8 RAM Chip are needed to provide a memory capacity of 2048 bytes including one ROM Chip of 512x8. Diagrammatically explain the memory connection to the CPU. (6)
- Q9 (a) What is mapping? Explain three types of mapping procedure used in transformation of data from main memory to cache memory. (6.5)
- (b) A computer use RAM chip of 1024x1 capacity. (6)
- (i) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
- (ii) How many chips are needed to provide a memory capacity of 16K bytes? Explain how the chips are to be connected to the address bus.

BCA-203
P2/2