(Please write your Exam Roll No.) Exam Roll No.

END TERM EXAMINATION

(16)

THIRD SEMESTER [BCA] DECEMBER-2012

Paper Code: BCA203 *Subject: Computer Architecture*

Time : 3 Hours *Maximum Marks :75*

Note: Attempt any five questions. Select one question from each unit including Q.no.1 which is compulsory.

Q1 (a) Define the Register Transfer language with example. **(5x5=25)**
(b) Draw the circuit of Binary Adder-Subtractor and explain its working.
(c) Explain the working of cache memory.
(d) Define the Direct and Indirect address.
(e) What is the difference between Microprocessor and Micro program?

UNIT-I

Q2 (a) Explain the hardware implementation of logic micro operation for AND, OR, XOR and complement logic gate. **(6.5)**
(b) Describe Three State Bus Buffer. Draw the diagram three state buffer. **(6)**

Q3 (a) Explain the circuit of accumulator logic. **(6.5)**
(b) Define the Instruction Cycle. Draw the flowchart for instruction cycle. **(6)**

UNIT-II

Q4 (a) Explain the stack organization. Write the algorithm for PUSH and POP. **(6.5)**
(b) Convert the following arithmetic expressions from infix to reverse polish notation:- **(6)**
(i) (A+B)*[C*(D+E)+F] (ii) A+B+A*(B*D+C*E)

Q5 (a) Evaluate the arithmetic statement X=(A+B)*(C+D) using zero, one, two or three Address Instruction. **(6.5)**
(b) What is pipeline? Explain the arithmetic pipeline. **(6)**

UNIT-III

Q6 (a) Design an array Multiplier that Multiplies two 4-bit number. **(6.5)**
(b) Define the following:- **(6)**
(i) Priority Interrupt (ii) Daisy-chaining priority

Q7 (a) Describe the different types of Mode of transfer. **(6.5)**
(b) Explain the DMA controller with the help of Block Diagram. **(6)**

UNIT-IV

Q8 (a) Explain Memory Hierarchy in a computer system. **(6.5)**
(b) A computer use RAM chip of 1024x1 capacity. **(6)**
(i) How many chips are needed for providing a capacity of 1024 bytes?
(ii) How should their Address Lines be connected to provide a memory capacity of 1024 bytes?

Q9 What is Mapping? Explain the all Mapping Methods (Associative Mapping, Direct Mapping and Set-Associative Mapping). **(12.5)**

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