Kamal Kundra

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END-TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER-2007

Paper Code: BCA-203(Batch-2005-2006) Subject: Computer Architecture
Paper ID: 20203

Time : 3 Hours Maximum Marks : 75

Note: Q.No.1 is compulsory. Attempt one question from each unit.

Q.1 (a) What do you mean by register transfer language (RTL)? (3)

(b) What are shift registers? Where are these useful? (3)

(c) What is Instruction Cycle? What are its types? (4)

(d) What is associative memory? Outline its significance. (3)

(e) What is stack organization? (3)

(f) What are I/O interfaces? How are these important? (3)

(g) What kind of hardware is required for memory management? Discuss. (3)

(h) What is the relevance of priority interrupt? (3)

Unit-I

Q.2 What are micro-operations? What are its various types? Illustrate the implementation of each category of micro-operations through its block diagram(s). (12.5)

Q.3 (a) What is a bus? Design a bus system capable of transmitting data from any register from a group of 16 registers (32-bits each) to any other register existing in a group of 8 registers (32-bits each). Illustrate the logic through its block diagram. (7.5)

b) What is the importance of timing and control in the design of control unit? (5)

Unit-II

Q.4 (a) What do you understand by an Instruction Set? What are different types of instructions? Discuss the significance of each type of instruction. (7)

b) What are addressing modes? Discuss different types of addressing modes. (5.5)

Q.5 Explain the following:

(a) Instruction Format (6)

(b) ALU Design (6.5)

Unit-III

Q.6 Explain the following: (6)

(a) Division algorithm

(b) Direct Memory Access (DMA) (6.5)

Q.7 (a) What is a floating point number? What maximum and minimum floating-point number can be represented in a 64-bit computer having a sign bit for mantissa, 15 exponent bits and 32 mantissa bits? Also indicate the positive/negative overflow and underflow ranges of the number on the scale. (9)

(b) Differentiate between synchronous and asynchronous data transfer. (3.5)

Unit-IV

Q.8 What is memory hierarchy? Discuss each of the elements in this hierarchy. (12.5)

Q.9 Differentiate between the following:

(a) RAM and ROM (6)

(b) Cache Memory and Virtual Memory (6.5)

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END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER-2008

Paper Code: BCA203 **Subject: Computer Architecture**
Paper Id: 20203 **(Batch: 2005-2007)**
Time : 3 Hours **Maximum Marks :75**

Note: Q.1 is compulsory. Attempt one question from each unit.

Q1 (a) What is wrong with the following register transfer statements? **(5)**

(i) $xT : AR \leftarrow \overline{AR},\ AR \leftarrow 0$ (ii) $yT : R1 \leftarrow R2,\ R1 \leftarrow R3$

(b) What do you understand by the branch and save return address? **(5)**

(c) Explain the Indexed addressing mode. **(5)**

(d) What is the difference between isolated I/O and memory mapped I/O? Also, explain the advantages and disadvantages of each. **(5)**

(e) What is memory hierarchy in a computer system? **(5)**

UNIT-I

Q2 (a) Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. **(4.5)**

(b) Design an arithmetic circuit with one selection variable S and two n-bit date inputs A and B. The circuit generates the following four arithmetic operation in conjunction will the input carry C_{in}. Draw the logic diagram for the first two stages. **(8)**

S	Cin=0	Cin=1
0	D=A+B	D=A+1
1	D=A-1	D=A+ $\overline{B}$ +1

Q3 (a) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? **(4.5)**

(b) Draw the block diagram of control unit of basic computer and explain. **(8)**

UNIT-II

Q4 (a) Draw full adder and explain its logic circuit. **(4.5)**

(b) What are the various phases of an instruction cycle? Give the microoperations of fetch and decode phases. How the first two register transfer statements are implemented? **(8)**

Q5 (a) What is the reverse polish notation? Explain with an example. **(4.5)**

(b) Write down a program to evaluate $Z = (A+B)*(C+D)*(G+H)$ by using three address instructions and zero address instructions. **(8)**

UNIT-III

Q6 (a) What do you understand by the divide overflow? **(4)**

(b) Show the contents of registers E, A, Q and SC during the process of multiplication of two binary numbers, 11111 (multiplicand) and 10101 (multiplier). The signs are not included. **(8.5)**

Q7 (a) Draw a block diagram for the DMA system showing the essential elements needed for the DMA transfer in a computer system. **(4.5)**

(b) Explain the difference between the daisy chaining priority and parallel priority interrupts. Draw the diagrams to explain their working. **(8)**

UNIT-IV

Q8 (a) Explain the concept of virtual memory. What are its advantages? **(4.5)**

(b) What is associative memory? Give and explain its architecture. **(8)**

Q9 (a) Explain the differences between cache and auxiliary memory. **(4.5)**

(b) A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is128Kx32. **(8)**

(i) Formulate all pertinent information required to operate the cache memory.

(ii) What is the size of the cache memory?

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END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER-2009

Paper Code: BCA203 Subject: Computer Architecture
Paper Id-20203

Time : 3 Hours Maximum Marks :75

Note: Q.1 is compulsory. Attempt one question from each unit.

Q1 Attempt **any ten** from the following:- (10x2.5=25)

(a) Draw the block diagram for the hardware that implements the following statements: x+yz : AR←AR+BR., where AR and BR are two n-bit registers and x, y and z are control variables.

(b) Design a 4-bit combinational circuit decrementer using four full adders.

(c) What are the two instructions needed in the basic computer in order to set the E flip flop to 1?

(d) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part. Draw the instruction word format and indicate the number of bits in each part.

(e) Write any three functions of stack.

(f) Why does DMA have priority over CPU when both request a memory transfer?

(g) Define overflow. How can we detect overflow?

(h) Give two advantages of booth multiplication.

(i) List various resistors with their functions required for basic computer function.

(j) (i) How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(ii) How many lines of address bus must be used to access 2048 bytes of memory?

(k) A ROM chip of 1024x8 bits has four select inputs and operates from a 5-volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.

(l) Define hit ratio.

UNIT-I

Q2 (a) Tabulate various shift micro operations and design a 4 bit combination circuit shifter. (5)

(b) The output of four registers R0, R1, R2, R3 are connected through 4-to-1-line multiplexers to the inputs of a fifth register, R5. Each register is eight bits longs. The required transfers are dictated by four timing variables T_0 through T_3 as follows:

T_0 : R5←R0
T_1 : R5←R1
T_2 : R5←R2
T_3 : R5←R3

Timing variables are mutually exclusive. Draw a block diagram showing the hardware implementation of the register transfers. (5)

(c) Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left followed by a shift-right and a circular shift-left. (2.5)

P.T.O.

Q3 (a) Describe the hardware implementation of logic micro operation. Draw the diagram of one stage of logic circuit used with AND, OR, NAND and XOR gates. **(5)**

(b) What is the difference between a direct and indirect address instruction? **(5)**

(c) Give a suitable example to discuss insert operation. **(2.5)**

UNIT-II

Q4 (a) Design a flow chart showing instruction cycle and interrupt cycle for basic computer operation. **(5)**

(b) Tabulate various memory reference instructions. Explain BUN and BSA. **(5)**

(c) Giving suitable block diagram show major components of CPU. **(2.5)**

Q5 (a) Illustrate the influence of number of address on X=(R+S)(U+V) using three address , two address and zero address instruction. **(5)**

(b) What is stack organization? Describe its function using a suitable example. Define stack limit. **(5)**

(c) What is the difference between implied and immediate addressing modes? **(2.5)**

UNIT-III

Q6 (a) Design and discuss 2 bit by 3 bit array multiplier. Give its major advantages. **(5)**

(b) Taking multiplicand 11111 and multiplier 01001 design a table of multiplication with booth multiplication algorithm. **(5)**

(c) Give register configuration for hardware implementation of signed 2's compliment addition/subtraction. **(2.5)**

Q7 (a) What do you understand by hand shaking? Discuss using suitable diagram:

(i) source initiated transfer using hand shaking.

(ii) Destination initiated transfer using hand shaking. **(5)**

(b) What is priority? Name various types of priority. Discuss Daisy chaining priority in brief. **(5)**

(c) List four peripherals devices that produce an acceptable output for a person to understand. **(2.5)**

UNIT-IV

Q8 (a) What is mapping? Name various types of mapping. Discuss direct mapping in brief. **(5)**

(b) Write a short note on memory hierarchy. **(5)**

(c) A computer uses RAM chips of 1024x1 capacity. **(2.5)**

(i) How many chips are needed to provide a memory capacity of 1024 bytes?

(ii) How many chips are needed to provide a memory capacity of 16K bytes?

Q9 (a) Giving suitable block diagrams differentiate between RAM and ROM. **(5)**

(b) Write a short note on Auxiliary memory. **(5)**

(c) Draw a block diagram of Associative memory. **(2.5)**

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