

END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE 2014

Paper Code: BCA-106

Subject: Digital Electronics (New)
(2011 Onwards)

Time: 3 Hours

Maximum Marks: 75

Note: Attempt any five questions including Q.No.1 which is compulsory.
Select one question from each unit.

Q.1

- (a) Explain Diode and Transistor as a switch with diagram and table. Give their merits. (5)
- (b) Implement Ex-OR gate using universal logic gates only. (5)
- (c) Explain Binary divider using successive subtraction method. (5)
- (d) What are the applications of Gray codes and excess-3 codes? (5)
- (e) What are the advantages of PROM as compared to PLA and PLD? (5)

UNIT - I

Q.2

- (a) Convert $A.B.C + \bar{A}.C$ expression into standard SOP form and standard POS. (6)
- (b) Prove $A=(BCD)=(A+B)(A+C)(A+D)$ using Boolean laws. Also give steps to solve Boolean expressions using K-map. (6.5)

Q.3

- (a) What is a logic family? Differentiate TTL and CMOS in terms of current & voltage parameters, Noise margin, fan-in fan-outs. (6.5)
- (b) Implement $Y=(AB)+A+BC$ Using NAND gates and NOR gates only. (6)

UNIT - II

Q.4

- (a) Show how a full adder can be converted to a full subtractor with the addition of an inverter circuit. (6)
- (b) Explain 4-bit carry look ahead adder in detail. (6.5)

Q.5

- (a) (i) Explain briefly the BCD to seven segment decoder. (3.5)
- (ii) How does an encoder differ from a de-multiplexer? Give advantages of each. (3)
- (b) Draw the logic diagram of parity generator/ checker. Explain its operation with the help of truth table. (6)

UNIT - III

Q.6

- (a) Differentiate:
 - (i) Combinational and sequential logics. (3)
 - (ii) Positive and negative edge triggering. (3)
- (b) Explain realization of JK flip-flop using D flip-flop. Also give four basic applications of flip-flops. (6.5)

Q.7

- (a) Explain Bidirectional shift register using four D flip-flops and four input multiplexers with timing diagram. (7)
- (b) Draw the logic diagrams of serial to parallel data transfer register using JK flip-flop synchronous inputs. (5.5)

UNIT - IV

Q.8

- (a) Design a MOD-10 up-down counter. (6)
- (b) How does the architecture of a PAL differ from a PROM? List the applications of PLAs. (6.5)

Q.9

- (a) Draw the logic diagram of 4-bit binary ripple counter using Flip-flops that trigger on negative-edge transition of clock, with clock cycle. (6.5)
- (b) Explain SRAM and DRAM with diagrams. (6)

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