(Please write your Exam Roll No.)

Exam Roll No. 01414202012

END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE-2013

Paper Code: BCA106	Subject: Digital Electronics (New)
Time : 3 Hours	Maximum Marks :75
Note: Attempt any five questio	ns including Q.no.1 which is compulsory.

Select one question from each unit.

Q1.	(a)	Design a Full Adder circuit using only NANAD gates only.	(5)
	jbt-	State and explain the DeMorgen's theorem which converts a sum into a product fr and vice versa.	rom (5)
	67	What is Multiplexer? Explain the difference between MUX and DEMUX.	(5)
	(d)	Explain Binary Multiplier.	(5)
(6.6)	(e)	Simplify the following function in Sum of product from using four variable Karnaug map. Draw the resulting logic diagram.	sh's (5)
Cale		F(A,B,C,D) = Σ (0,1,2,4,5,7,11,15)	
(c) • ;		Unit- I	
Q.2.	(a)	(i) Simplify the Expression AB + \overline{AC} + \overline{ABC} (AB+c)	(3)
		(ii) Simplify the given Boolean Expression	(3)
		$Y = \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC}$	
	(b)	Explain what is meant by logic family. Describe three major difference between RT DTL.	L and (6.5)
Q.3.	(0)	Explain how the basic gates can be realized using NAND gates. Draw the useful	
		Diagram.	(6.5)
	1bt	Implement $Y = AB + A + B + C$ using NAND gates only.	(6)
		Unit – II	
Q.4	(a)	Draw a Multiplexer using only NAND gates which selects from four inputs A0 to A3	
		using two select inputs SO and S1.	(6.5)
	(b)	Implement the following function using a Multiplexer	

P.T.O.

		[-2-]	.*
		$F(A,B,C) = \Sigma(1,22,5,6)$	(6)
Q5.	(a)	How does an encoder differ from decoder? Design 3 X 8 decoder.	(6.5)
	(b)	Design a 4 bit parallel binary adder.	(6)
		Unit- III	
Q.6.	(a)	Explain in detail the construction and working universal / Bidirectional shift regist	er. ´(6)
5	(b)	Explain the operation of Master - slave Flip Flop and show how the race around	
		condition is eliminated in it?	(6.5)
Q7.	(a)	Explain the function of a D flip flop using a suitable diagram and discuss how it w	orks as
		a latch?	(6)
J. y	(b)	How an SR flip flop can be converted into JK flip flop? Give the truth table of JK fl	ip flop
249	ierrea p	Flop:	(6.5)
		Unit-IV	
08	(a)	Design a MOD 7 binary counter. Draw its state diagram and circuit.	(6)
	(b)	What is a modulus counter? Draw the logic diagram of a 4 bit binary ripple count	er using
		flip-flops that trigger on the positive edge transition.	(6.5)
			. *.
Q.9.	(a)	What is ROM? Explain the terms volatile memory and non-volatile memory.	(6)
Lang.	(b)	What is a ripple counter? Explain the difference the performance of asynchronou	is and

(6.5)

[-2-]

12 BARE

synchronous counter.

Download Study Material from StudentSuvidha.com