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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-2010

Paper Code: BCA 106	*Subject: Digital Electronics*
Paper ID: 20106	
Time : 3 Hours	*Maximum Marks : 75*

Note: Question 1 is compulsory. Attempt one question from each unit.

Q1. (a) Show the universality of NAND and NOR gates. Use them to implement the 'inverter', 'and'; 'or' logic operations. **(5)**

(b) State the Morgan's theorem and show that **(5)**

$\overline{ABC} = A + \overline{B} + C$ *and* $\overline{(A + B + C)D} = \overline{A}\ \overline{B}\ \overline{C} + \overline{D}$

(c) Explain the working of a half subtractor. Show logic circuit. **(5)**

(d) Sketch waveforms of clock pulses and output of three flip flops of a asynchronous 3 bit ripple counter. **(5)**

(e) Draw logic circuit and truth table of a 2 to 1 multiplexer and show how one of the two inputs are selected. **(5)**

UNIT-I

Q2. (a) Explain the rules of addition, subtraction and multiplication of binary numbers (with examples). **(6.5)**

(b) Prove A +A = A; A+AB =A; AA= A **(3)**

(c) Show that : $X = \overline{A}B + A\overline{B} + AB + \overline{A}\,\overline{B} = 1$ **(3)**

$X = A + \overline{A}B + \overline{A}\,\overline{B} = 1$

Q3. (a) Simplify the following Boolean- expressions. **(6.5)**

(i) $X = AB\overline{C} + \overline{A}BC + A\overline{B}\,\overline{C} + A\overline{B}C + \overline{A}BC$

(ii) $(A + \overline{B})\ (BB + C)$

(b) Construct logic circuits that can implement the following expressions: **(6)**

(i) $X = AB + \overline{B}C$

(ii) $X = (AB + C)D$

UNIT-II

Q4. Define the function of a multiplexer and demultiplexer in digital circuits. Draw neat logic circuits and truth table of a simple demultiplexer. **(12.5)**

Q5. Explain the working of a half adder. Show logic circuit, B. expression and truth table. How will the circuit behave if NOT gate is removed? **(12.5)**

UNIT-III

Q6. (a) Define hatch and differentiate between a hatch and flip- flop. **(6.5)**

(b) Draw and explain master- slave JK flip flop. **(6)**

Q7. (a) Explain serial-in-serial-out shift register. **(6.5)**

(b) Design a 2X4 decoder circuit. **(6)**

UNIT-IV

Q8. Draw the logic circuit and explain a 4 bit ripple counter. Show the type of flip flops used and explain the counting process. **(12.5)**

Q9. (a) Describe the semiconductor/ magnetic/ optical memory devices used in computer systems. **(4.5)**

(b) Explain (i) Static and dynamic RAM. **(8)**

(ii) ROM, PROM, EPROM

Differentiate between them and give applications.

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-2008

Paper Code:BCA-106 **Subject: Digital Electronics**
Paper Id:20106 **Batch (2005-2007)**

Time : 3 Hours **Maximum Marks :75**

Note: Q1. is compulsory. Attempt one question from each part.

Q1. (a) State and explain the DeMorgan's theorem which convert a sum into a product form and vice-versa. (5)

(b) Design a full adder circuit using only NOR gates. What relations has it to the half-adder circuit. (5)

(c) What is a demultiplexer? Explain the difference between a DEMUX and MUX. (5)

(d) Discuss the difference between combinational and sequential logic. (5)

(e) Why are shift registers considered to be basic memory devices? (5)

PART-A

(12.5)

Q2. (a) Express the function Y = A+ $\overline{B}$ C in (a) Canonical SOP and (b) Canonical POS form.

(b) Explain the terms: (i) prime implicant (ii) input variable (iii) minterm and (iv) maxterm

Q3. (a) Realise (i) $Y = A + BC\overline{D}$ using NAND gates and (12.5)

(ii) $Y = (A + C)(A + \overline{D})(A + B + \overline{C})$ using NOR gates

(b) Realise the following function using (i) multilevel NAND-NAND network and (ii) multilevel NOR-NOR network.

$$Y = \overline{A}B + B(C + D) + E\overline{F}(\overline{B} + \overline{D})$$

PART-B

Q4. (a) Show how a full adder can be converted to a full subtractor with the addition of an inverter circuit. (12.5)

(b) Explain (i) 1-to-8 demultiplexer (ii) 1-to-16 demultiplexer.

Q5. (a) Design a parallel binary multiplier that multiplies a 4-bit number $B=B_3B_2B_1B_0$ by a 3 bit number $A=A_2A_1A_0$ to form the product $C=C_6C_5C_4C_3C_2C_1C_0$. (12.5)

(b) Draw the logic diagram of IC74180 parity generator/checker and explain its operation with the help of a truth table.

PART-C

Q6. (a) Explain the function of a D flip-flop using a suitable diagram and discuss how it works as a latch? (12.5)

(b) Show that a J-K flip-flop can be converted to a D flip-flop with an inverter between the J and K inputs.

Q7. (a) Explain the operation of master-slave flip-flop and show how the race around condition is eliminated in it? (12.5)

(b) What is the major difference in the operation of edge-triggered flip-flops and master-slave flip-flops?

PART-D

Q8. (a) What is a ripple counter? What factors determine whether a counter operates as a count-up or count-down counter? (12.5)

(b) What is a modulus counter? Draw the logic diagram of a 4 bit binary ripple counter using flip-flops that trigger on the positive-edge transition.

Q9. (a) What is a ROM? Explain the terms: (a) Volatile memory (b) Non Volatile memory. (12.5)

(b) Describe and compare sequential access memories, random access memories and read only memories.

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY 2008

Paper Code:BCA-106 **Subject: Digital Electronics**
Paper Id:20106 **Batch (2001-2004)**
Time : 3 Hours **Maximum Marks :75**

Note: Attempt any five questions.

Q1. (A) Realize (Draw the logic diagram) for the following. (8)
(a) x'y' + xy
(b) AC + AB'
(c) (x'+y)'
(d) (x+y+z') (x'+y'+z')
(e) (AB'C'D) + AB'C'

(B) Find the equivalent of following equations. (7)
G= u+vw'+x(y'+z)'

Q2 (a) Simplify the following four variable equations: (8)
K = f(w,x,y,z) = Σ (0, 1, 4, 5, 9, 11, 13, 15)

(b) Design a 4 bit look-ahead adder circuit. Discuss the functionality of it. (7)

Q3. (a) Design a two bit binary multiplier. (8)
(b) Design a 4 bit multiplexer using AND-OR gates. (7)

Q4. (a) Define hatch. Differentiate between hatch and flip flop. (8)
(b) Draw and explain master slave J-K flip flop. (7)

Q5. (a) Draw and explain 4 bit ripple counter. (8)
(b) Design a mod-10 up counter. (7)

Q6. (a) Explain serial-in-serial-out shift register. (8)
(b) Design 2x4 decoder circuits. (7)

Q7. Write short notes on (any two): (15)
(a) RTL
(b) CMOS Logic
(c) EROM

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END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY - JUNE 2007

Paper Code:BCA-106 **Subject: Digital Electronics (2005 Batch)**

Time : 3 Hours **Maximum Marks :75**

Note: Question No. 1 is compulsory. Attempt four questions from the remaining paper, selecting one question from each part.

Q1. (a) Find out the value of the following.

(i) $(11010010)_2 = (X)_8$ (1)

(ii) $(AB)_{16} = (X)_2$ (1)

(b) Fill in the blanks

(i) _____ gate does not take part in logical operation. (1)

(ii) The _____ and _____ gates are universal gates. (1)

(iii) The gate _____ generates transfer function of applied input. (1)

(c) Simplify the following Boolean function and draw logical circuit. (5)

$F(A, B, C, D) = \Sigma (0, 6, 8, 13, 14)$

$D(A, B, C, D) = \Sigma(2, 4, 10)$

(d) Design 3-bit binary counter using T flip-flop. (5)

(e) Sum of all minterms of a Boolean function of n variables is 1. Prove this statement for n=3. (5)

(f) Construct a master-slave flip-flop using two R-S flip-flops. (5)

PART-A

Q2. (a) Design a combinational circuit whose input is a three bit number and whose output is 2's complement of the number. (7)

(b) Explain why NOR and NAND gates are universal gates. (5.5)

OR

Q3. (a) Design a 4-bit binary to gray code converter. (7)

(b) Design a BCD to Excess-3 code converter with a BCD-to-Decimal decoder and four OR gates. (5.5)

PART-B

Q4. (a) Explain a parallel binary adder with the help of logical diagram and sum two binary numbers A = 1101 and B=1001 using parallel binary adder. (7)

(b) Explain a full adder circuit and construct it with the help of a 3 X 8 Decoder and two OR gates. (5.5)

OR

Q5. (a) Design sequential circuit for the following state table using 2-bit register and combinational gates. (7.5)

Present State		INPUT	NEXT STATE	
A	B	X	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

(b) Construct a half Adder circuit using basic gates (AND, OR, NOT) only. (5)

PART-C

Q6. (a) A flip-flop has 20-ns delay from the time its CP input goes from 1 to 0 to the time the output is complemented. Find out the followings. (5)

(i) What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops?

(ii) What is the maximum frequency at which the counter can operate reliably?

(b) Explain shift register and different configurations of shift register. (7.5)

OR

Q7. (a) Why J-K flip-flops is known as universal flip-flop. Design a T-flip-flop and D-flip-flop using J-K flip-flop. (7)

(b) Design a logical diagram of a 32 x 4 ROM. (5.5)

PART-D

Q8. (a) Explain look-ahead carry generator and design logical diagram of a look-ahead carry generator. (7.5)

(b) Explain multiplexer and implement it to the following Boolean function using 4 x 1 multiplexer. (5)

$F(A, B, C) = \Sigma (1, 3, 5, 6)$

OR

Q9. (a) Design a combinational circuit that accepts a two bit number and generates a binary number equal to the square of the input number. (7.5)

(b) Write short notes on **any two** of the followings. (5)

(i) Encoder

(ii) Sequential Circuit

(iii) Edge-Triggered-Flip-Flop

(iv) Demultiplexers