Roll No. :....

Time: Three Hours]

24487

B. Tech. 7th Semester (CSE) Examination – May, 2015

ADVANCED COMPUTER ARCHITECTURE

Paper: CSE-401-F



[Maximum Marks: 100

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note: Attempt five questions in all. Q. No. 1 is compulsory. Select one question from each Unit.

- 1. (a) What is pipelined processor? Explain.
 - (b) What is On-Chip caches?
 - (c) What is memory module?
 - (d) What is multiple issue machines?
 - (e) What is virtual caches? Explain.

24487-1,700-(P-3)(Q-9)(15)

P. T. O.

SECTION - A

- **2.** (a) Write and explain various phases of processor project? Explain.
 - (b) Explain processor evaluation matrix.
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- 3. (a) Explain different type of instruction set.
 - (b) Describe three level of addressing.

SECTION - B

- 4. (a) What do you mean by Two-Level Caches?

 Explain.
 - (b) Explain different type of traffic created by instruction.
- 5. (a) Describe Split-I-and D-caches.
 - (b) An integrated cache with two reference per instruction (one I reference and, one D reference).
 The data (D) references are divided: 68% reads,
 32% writes 30% Dirty Lines, 8B Physical word,
 64B line, 5% Read miss rate. Compute the memory traffic for a 5% miss rate for each.

24487-1,700-(P-3)(Q-9)(15) (2)

SECTION - C

- **6.** Explain models of multiple simple processors and memory.
- **7.** (a) How to determine the waiting time, relative performance and buffer size? Explain.
 - (b) Describe Open-Queue memory model in details.

SECTION - D

- **8.** What is vector processor? Describe vector functional units.
- **9.** (a) What are the basic issues in multiprocessor? Explain.
 - (b) Explain memory coherence in shared memory multiprocessor.

