B.Tech.
Third Semester Examination
Digital Electronics (EE-204-F)

Note : Attempt any *FIVE* questions. All questions carry equal marks.

Q. 1. (a) Write the truth table and symbol of following gates :

(i) EX-OR,   (ii) NAND,   (iii) NOR.

Ans. EX-OR :

Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

A, B = inputs.

Y = Output

$$Y = A \text{ EX-OR } B$$
$$= A \oplus B$$
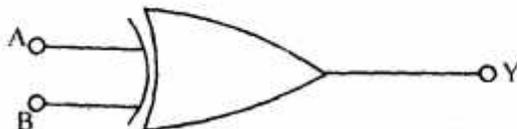
Standard symbol for EX-OR gate

(ii) NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Symbol :
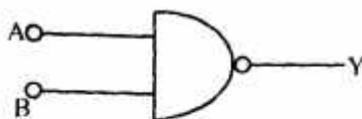
2 input NAND gate

(iii) NOR Gate :

A	B	Y
0	0	1
0	1	0

1

| I | 0 | 0 |
| I | 1 | 0 |

Symbol :
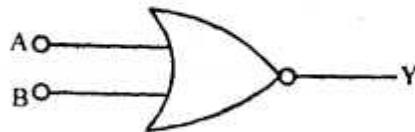
2 input NOR gate

Q. 1. (b) What is De-Morgan's theorem. Solve using this theorem to prove the following :

$$(A + B).(C + D) = \overline{\overline{(A + B)} + \overline{(C + D)}}$$

Ans. De-Morgan's Theorem :

$$\overline{A.B} = \overline{A} + \overline{B} \text{ and}$$

$$\overline{A + B} = \overline{A}.\overline{B}$$

Proof : Take RHS

$$\overline{\overline{(A + B)} + \overline{(C + D)}}$$

$$= \overline{\overline{(A + B)}.\overline{(C + D)}}$$

$$= (A + B).(C + D)$$

$$= \text{L.H.S.} \qquad\qquad \text{Hence proved.}$$

Q. 2. (a) Convert $(736)_8$ to binary.

Ans. Octal to binary

$$7 \rightarrow 111$$

$$3 \rightarrow 011$$

$$6 \rightarrow 110$$

$$(736)_8 = (111\ 011\ 110)_{20}$$

Q. 2. (b) Convert $(0.10100110)_2$ to octal.

Ans. $(0.10100110)_2 = (0.101\ 001\ 100)_2$

$$= (0.5 \quad 1 \quad 4)_8$$

$$= (0.514)_8$$

I

Q. 2. (c) Represent decimal numbers 27 in binary form using :

(i) **BCD Code**   (ii) **Excess-3 Code**

(iii) **Gray Code**

Ans. (i) BCD Code : 27

Each digit of the decimal number is coded using 4 bit BCD code as given below :

$$0010 \ 0111$$

(ii) Excess-3 Code : Each digit of decimal number is coded using 4 bit excess 3 code as,

$$0101 \ 1010$$

(iii) Gray Code : 5 bits are required to represent 27, therefore 5 bit gray code is constructed and 27 is rep

as

$$10110$$

Q. 3. (a) What are error codes?

Ans. In digital systems, a process of coding is employed whereby each numeral, alphabet or special character is coded in a unique combination of 0's and 1's using a coding scheme, known as code. The process of coding is known as encoding.

There can be a variety of coding schemes (codes) to serve different purposes, such as arithmetic operations, data entry, error detection and correction etc. In digital system, a large number of codes are in use. Selection of a particular code depends on its solvability for the purpose.

Q. 3. (b) Perform using 2's complement method :

(i) **0011.1001–0001.1110**

(ii) **01100 – 00011**

Ans. (i) 0011.1001–0001.1110 :

$$(0011.1001) + (-0001.1110)$$

$$(0011.1001) + (1110.0001)$$

```
  1 1         1
    0 0 1 1 . 1 0 0 1
 +  1 1 1 0 . 0 0 0 1
   ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾
  1) 0 0 1 1 0 1 0
```

Discharge

(ii) 01100 – 00011 :

$$(01100) + (-00011)$$

$$(01100) + (11101)$$

```
   1 1
 +  0 1 1 0 0
    1 1 1 0 1
   ‾‾‾‾‾‾‾‾‾‾
  1) 1 1 0 0 1
```

Discharge

$$= 11001 \text{ Ans.}$$

Q. 3. (c) Add :

(i) $1011 + 1101$

(ii) $1010.1100 + 101.01$

Ans. (i) $1011 + 1101$:

$$
\begin{array}{r}
111 \\
1011 \\
1101 \\
\hline
11000
\end{array}
$$

(ii) $1010.1100 + 101.01$:

$$
\begin{array}{r}
11111 \\
1010.1100 \\
+ \quad 0101.0100 \\
\hline
1.0000.0000 \quad \textbf{Ans.}
\end{array}
$$

Q. 4. (a) Minimize the four variable logic function using K-map :

$$f(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14).$$

Ans.
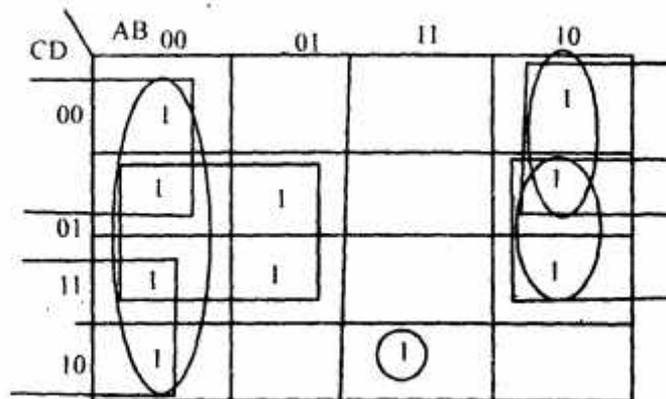
Pairs, $(8, 9, 0, 1), (11, 9, 1, 13), (5, 7, 3, 1), (2, 3, 1, 0)$

Hence, the minimized equation is

$$f(A, B, C, D) = ABC\overline{D} + \overline{B}\,\overline{C} + \overline{B}D + \overline{A}D + \overline{A}\,\overline{B}$$

Q. 4. (b) Design a full adder circuit and realize it.

Ans. Truth table of full adder.

| Inputs			Outputs	
A_n	B_m	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) S_n

(b) C_{n-1}
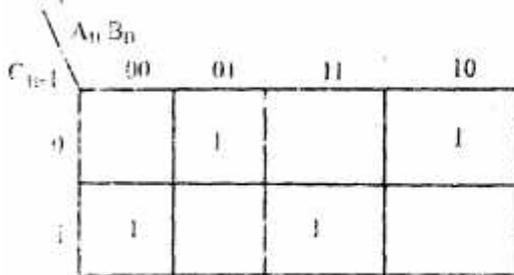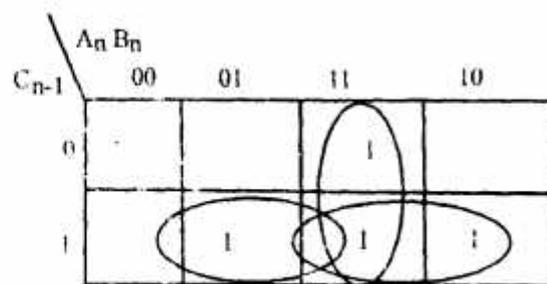
$$S_n = \bar{A}_n B_n \bar{C}_{n-1} + \bar{A}_n \bar{B}_n C_{n-1} + A_n \bar{B}_n \bar{C}_{n-1} + A_n B_n C_{n-1}$$

$$C_n = A_n B_n + B_n C_{n-1} + A_n C_{n-1}$$
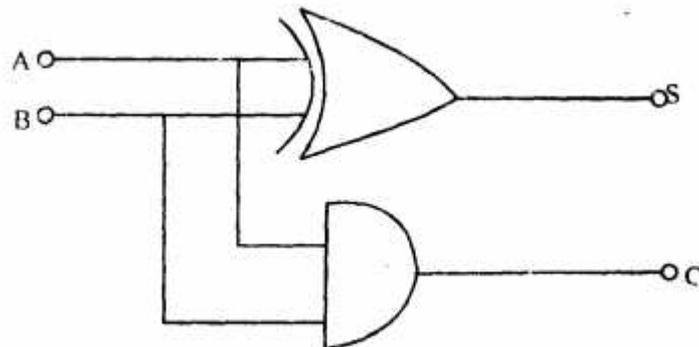
Realization of half adder
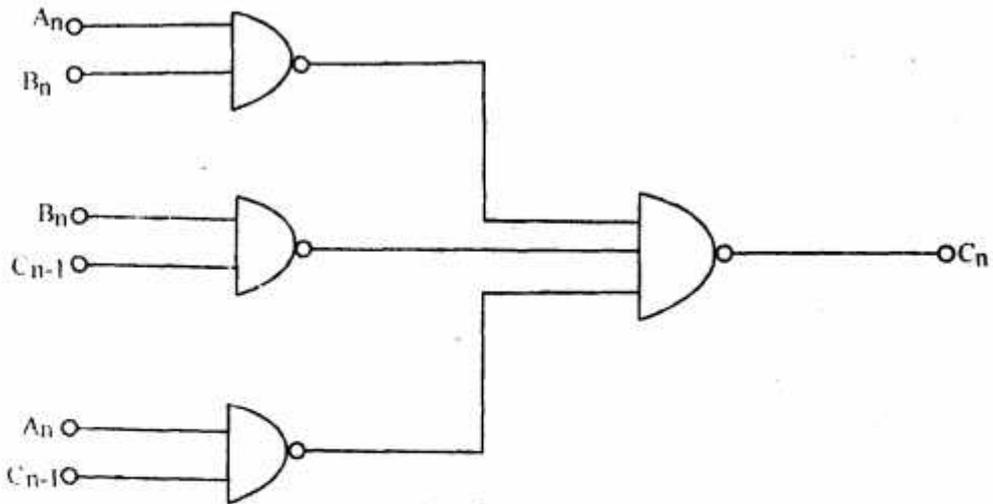
NAND realization for C_n

Q. 5. (a) Make a 32 : 1 MUX using two 16 : 1 MUX.

Ans.
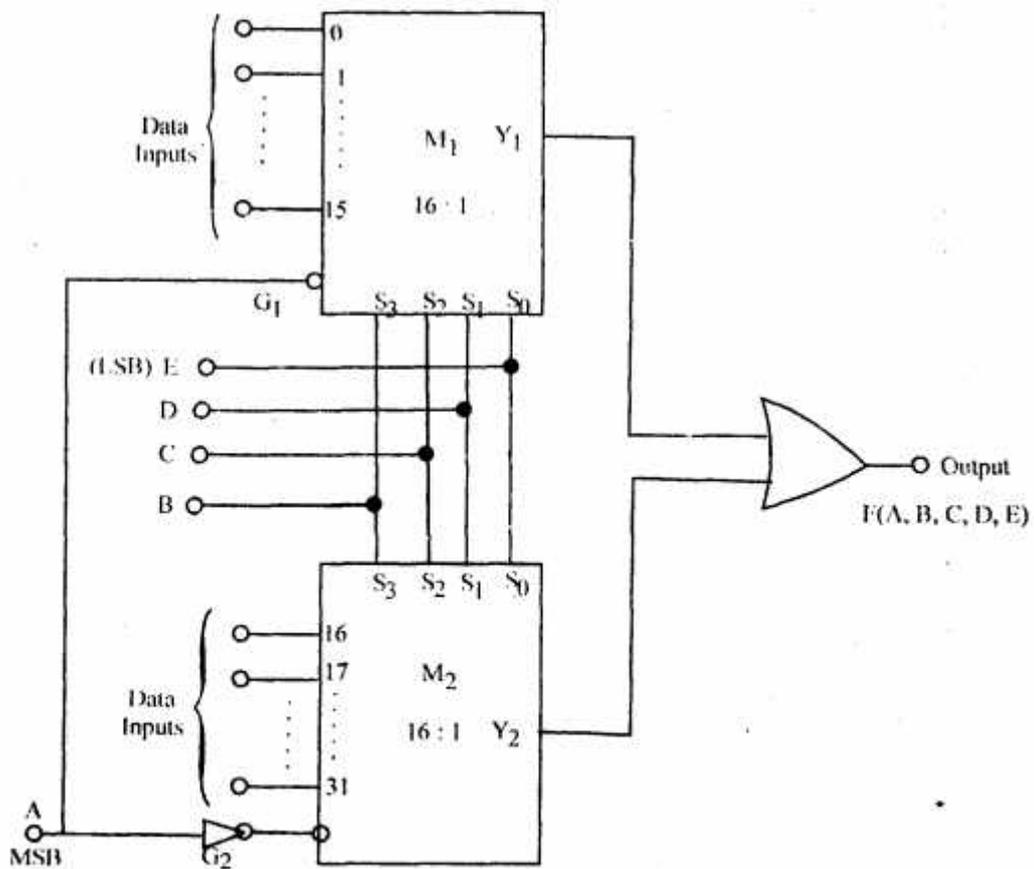
*32 : 1 Mux using two 16 : 1 mux and one OR gate*

Q. 5. (b) Explain the working of a Master-slave J-K flip flop.

Ans.
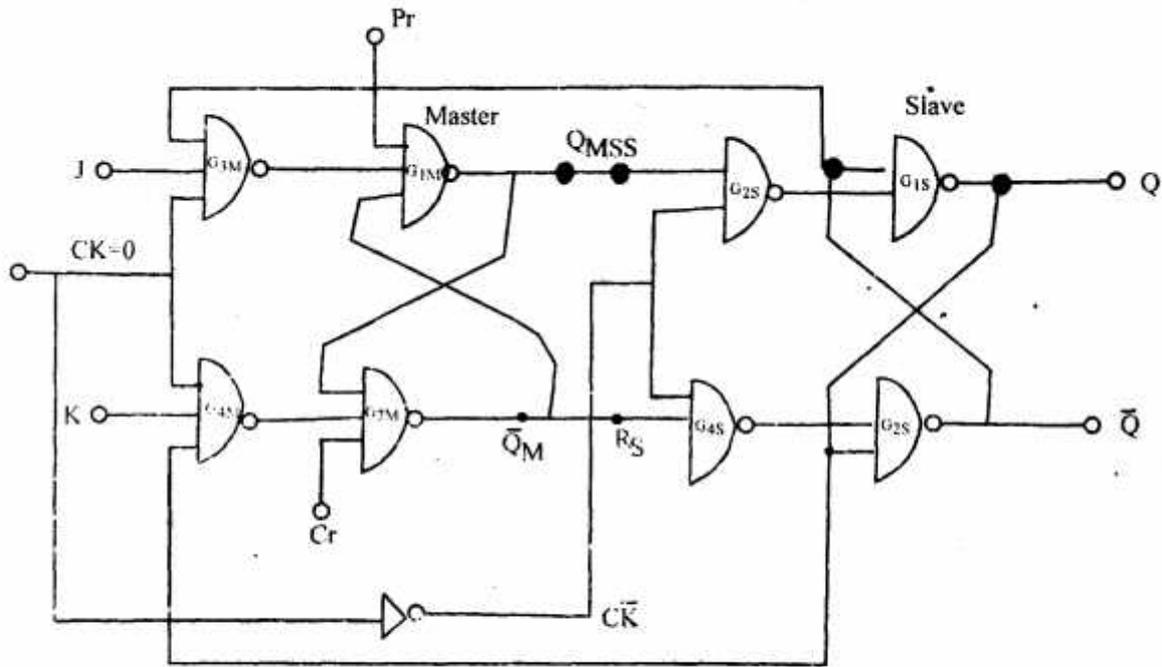
A master state JK flip-flop
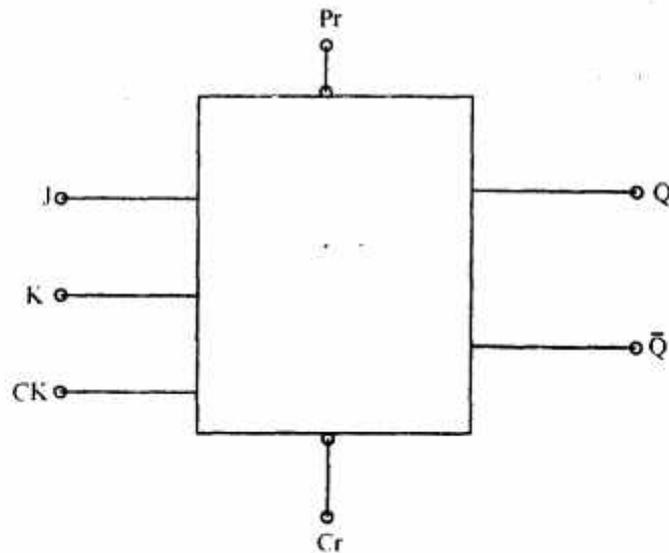
MS-JK F-F Logic symbol

A master slave JK F-F is a cascade of 2 SR flip-flops. With feedback from the outputs of the second to inputs of first as illustrated in fig. Positive clock pulses are applied to the first flip-flop and the clock pulse are

inverted before these are applied to the second flip-flop.

**Q. 6. Explain the following terms in logic families :**

(i) Speed of operation   (ii) Power dissipation

(iii) Figure of merit   (iv) FAN-OUT

Ans. (i) Speed of Operation : The speed of a digital circuit is specified in terms of the propagation delay time. The input and output waveforms of a logic gate are shown as :
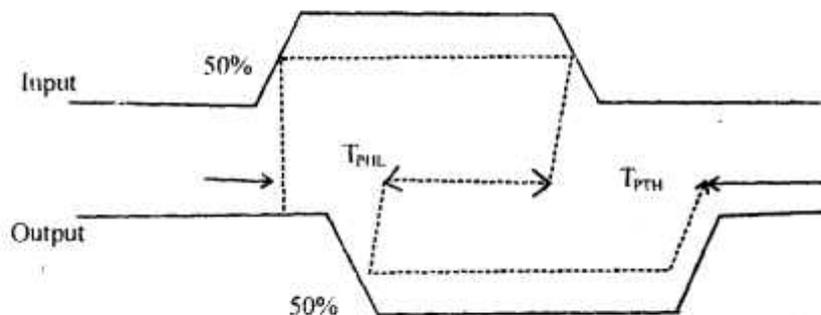
Input output voltage waveforms to define propagation delay times.

The delay times are measured between the 50 percent voltage levels of input and output waveforms.

There are two delay time : t_{PHL}, when the output goes from HIGH state to the LOW state and t_{PLH}, corresponding to the output making a transition from LOW state to the HIGH state.

The propagation delay time of the logic gate is taken as the average of these 2 delay times.

(ii) Power Dissipation : This is the amount of power dissipated in an IC. It is determined by the current, I_{CC}, that it draws from the V_{CC} supply, it is given by $V_{CC} \times I_{CC}$.

I_{CC} is the average value of $I_{CC}(0)$ and $I_{CC}(1)$. This power is specified in milliwatts.

(iii) Figure of Merit : It is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nano-seconds.

Figure of Merit = Propagation delay time (ns) * power (mw)

It is specified in pico-joules (ns * mw = pJ).

A low value of speed power product is desirable.

In a digital circuit, It is desired to have high speed, i.e., low propagation delay, then there is a corresponding increase in the power dissipation and vice-versa.

(iv) FAN-OUT : This is the number of similar gates which can be driven by a gate. High fan-out is advantageous because it reduces the need for additional drivers to drive more gates.

Q. 7. (a) Convert an S-R flip-flop to J-K flip-flop.

Ans. The uncertainty in the start of an S-R flip-flop when $S_n = R_n = 1$ (Fourth row of the truth table) can be eliminated of converting it into JK flip-flop.

The datas inputs are J and K which are ANDED with $\overline{Q}$ and Q respectively, to obtain S and R inputs, i.e.,

$$S = J.\overline{Q}$$

$$R = K.Q.$$

A J.K. flip-flop is obtained as :
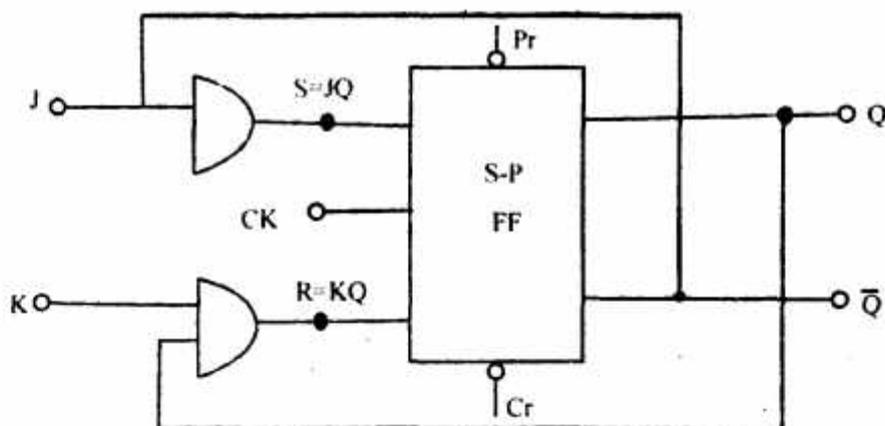
Data Input		Output		Input to SRFF		Output Q_{n1}	
J_n	K_n	Q_n	$\overline{Q}_n$	S_n	R_n	Q_{n+1}	
0	0	0	1	0	0	0	Q_n
0	0	1	0	0	0	1	
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	
1	1	0	1	1	0	1	Q_n
1	1	1	0	0	1	0	

Truth table of JK F-F.

Inputs		Outputs
J_n	K_n	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

Q. 7. (b) Design a 3 bit binary DOWN counter.

Ans. The number of flip-flops required is 3. Let the flip-flops FF_0, FF_1 and FF_2 are taken.

Flip-Flop	Inputs	Outputs
FF_0	J_0, K_0	Q_0
FF_1	J_1, K_1	Q_1
FF_2	J_2, K_2	Q_2

Counter state			Flip-flop inputs						
			FF$_0$		FF$_1$		FF$_2$		
Q_2	Q_1	Q_0	J_0	K_0	J_1	K_1	J_2	K_2	
0	0	0	1	×	0	×	0	×	
0	0	1	×	1	1	×	0	×	
0	1	0	1	×	×	0	0	×	
0	1	1	×	1	×	1	1	×	
1	0	0	1	×	0	×	×	0	
1	0	1	×	1	1	×	×	0	
1	1	0	1	×	×	0	×	0	
1	1	1	×	1	×	1	×	1	

K-maps:

0   0   0

$J_0 = 1$

$K_0 = 1$

$J_1 = Q_0$

$K_1 = Q_0$

$J_2 = Q_0 Q_1$

$K_2 = Q_0 Q_1$

Consider one column of the counter state at a time and apart from the first row.

The results are.

$$J_0 = 1$$
$$K_0 = 1$$
$$J_1 = Q_0$$
$$J_2 = Q_0 Q_1$$
$$K_1 = Q_0$$
$$K_2 = Q_0 Q_1$$

Q. 8. Write short notes on any two :

(a) Priority Encoders   (b) Johnson Counters

(c) Shift Registers   (d) TTL Logic Family

Ans. (a) Priority Encoders :

(i) Decimal to BCD Encoder

(ii) Octal to Binary Encoder

(i) Decimal to Binary CD Encoder : One of the most commonly used input device for a digital system is a set of 10 switches, one for each numeral between 0 and 9.

These switches generate 1 or 0 logic levels in response to turning them OFF or ON. When a particular number is to be fed to the digital circuit in BCD code, the switch corresponding to that number is pressed.
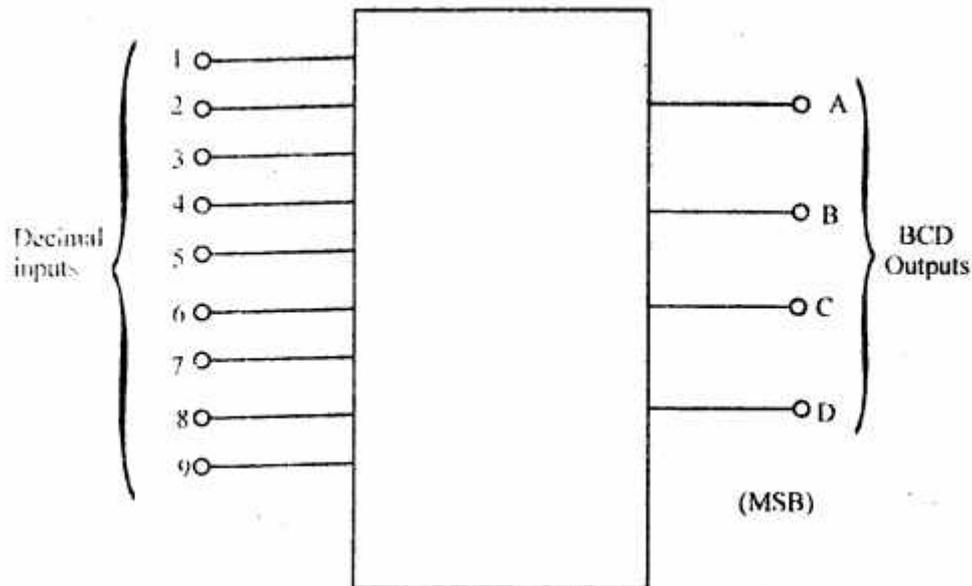
Block diagram of 74147 decimal to BCD priority encoder.

Truth Table of 74147

| Active low decimal inputs									Active low BCD outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
x	0	1	1	1	1	1	1	1	1	1	0	1
x	x	0	1	1	1	1	1	1	1	1	0	0
x	x	x	0	1	1	1	1	1	1	0	1	1
x	x	x	x	0	1	1	1	1	1	0	1	0
x	x	x	x	x	0	1	1	1	1	0	0	1
x	x	x	x	x	x	0	1	1	1	0	0	0
x	x	x	x	x	x	x	0	1	0	1	1	1
x	x	x	x	x	x	x	x	0	0	1	1	0

(ii) Octal to Binary Encoder : The octal code is often used at the input of digital circuits that require manual entering of long binary words. Priority encoder 74148IC has been designed to achieve this operation.
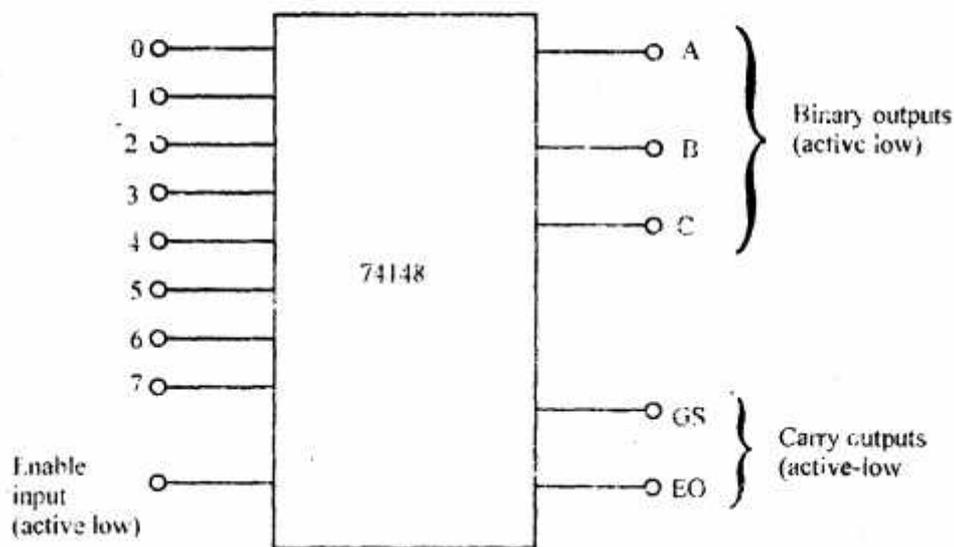
*Block diagram of 74148 octal to binary priority encoder*

Truth table of 74148

0	1	2	3	4	5	6	7	C		B	A	GS	EO	
1	x	x	x	x	x	x	x	x		1	1	1	1	1
0	0	1	1	1	1	1	1	1		1	1	1	0	1
0	x	0	1	1	1	1	1	1		1	1	0	0	1
0	x	x	0	1	1	1	1	1		1	0	1	0	1
0	x	x	x	0	1	1	1	1		1	0	0	0	1
0	x	x	x	x	0	1	1	1		0	1	1	0	1
0	x	x	x	x	x	0	1	1		0	1	0	0	1
0	x	x	x	x	x	x	0	1		0	0	1	0	1
0	x	x	x	x	x	x	x	0		0	0	0	0	1
0	1	1	1	1	1	1	1	1		1	1	1	1	0

(b) Johnson Counter : In a shift register, if $\overline{Q_0}$ is connected to the serial input, the resulting circuit is referred to as twisted ring, Johnson or Moebius counter.

If the clock pulses are applied after clearing the flip-flops, square waveform is obtained at Q outputs. Similar to ring counter sequence, the Johnson sequence is also useful for control state counters. It is also useful for the generation of multiphase clock.

The Johnson counter is a divide by 2N counter. For decoding the count, two input AND gates are required.

Output Waveform :

/
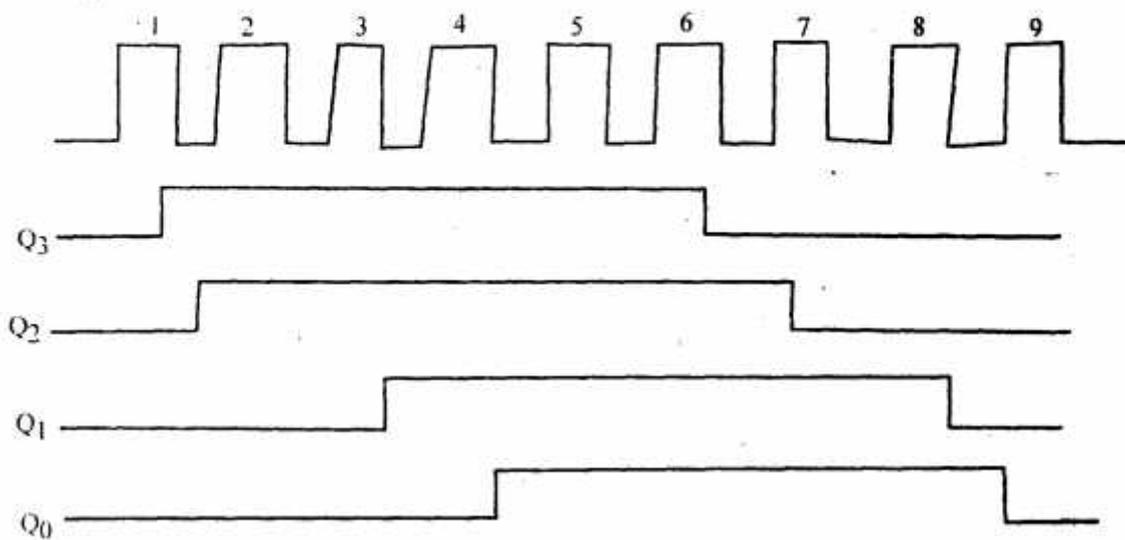
Johnson Counter (4 Bit) :
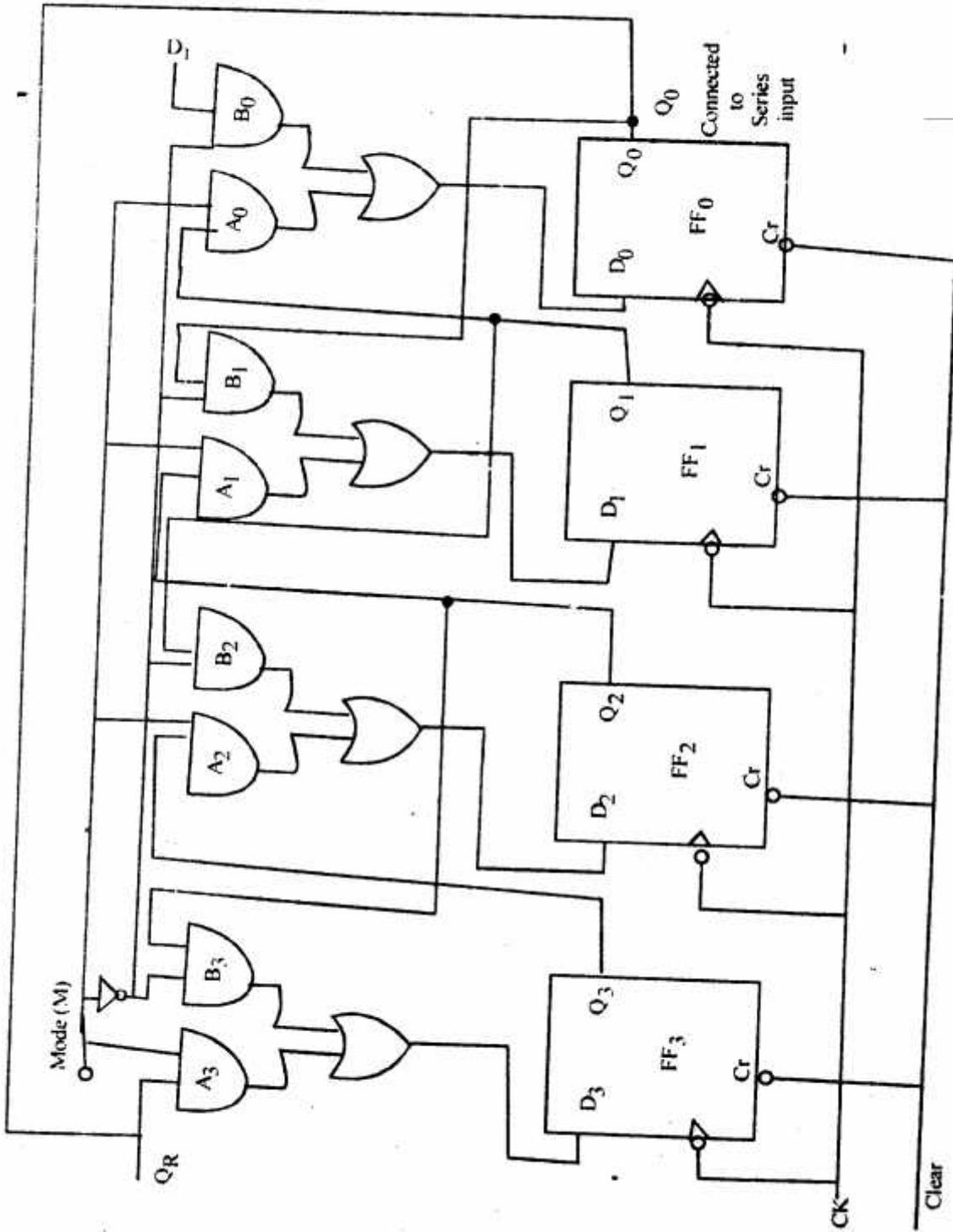
(c) Shift Registers : A shift register (5 bit) uses 5 master slave SR (or JK) flip-flops.

An array of flip-flops is required to store binary information, the number of flip-flops required being equal to the number of bits in the binary word (one FF for each bit) and is referred to as a register.

The data can be entered in serial (one bit at a time) or in parallel form (all the bits simultaneously) and can be retrieved in the serial or parallel form.

Data in serial form is also referred to as temporal code and in parallel form as spacing code.

Registers are classified depending upon the way in which data are entered and retrieved.

There are 4 possible modes of operations :

(i) Serial in serial out (SISO)

(ii) Serial in parallel out (SIPO)

(iii) Parallel in, Serial out (PISO)

(iv) Parallel in, Parallel out (PIPO)

Registers in which data are entered or/and taken out in serial form are referred to as shift registers since bits are shifted in the FFs with the occurrence of clock pulses either in the right direction (right shift register) or in left direction (left shift register).

In the bi-directional shift register, data can be shifted from left to right as well as in the rerverse direction, using the mode control.

For example, IC-74295A is a bidirectional shift register.

There are applications in which shifting data to the right and/or to the left is required. For example, a binary number can be divided by two by shifting it one stage to the right.

In this process, the least significant bit is lost causing an error of 0.5 if the no. is odd.

(d) TTL. Logic Family : Because of the speed limitations. TTL has become outdated and is completely replaced by another logic family referred to as transistor transistor logic (TTL). The main cause for the speed limitation in DTL is the slow process of retrieval of stored base charge of the output transistor.

For example, in the DTL gate, when T goes from saturation to cut off, the diodes D_1 and D_2 are non-conducting & hence the base charge must leak off through the resistor R_B, which is a relatively slow mechanism.

The operation of TTL gate is similar to the operation of DTL gate, as far as the steady state operation is concerned, as is evident.

For the operation discussed, we assume that the local gates are now present and the voltages for logic 0 and 1 are $V_{CT} \cdot Sat = 0.2\,V$ and $V_{CC} = 5V$ respectively.
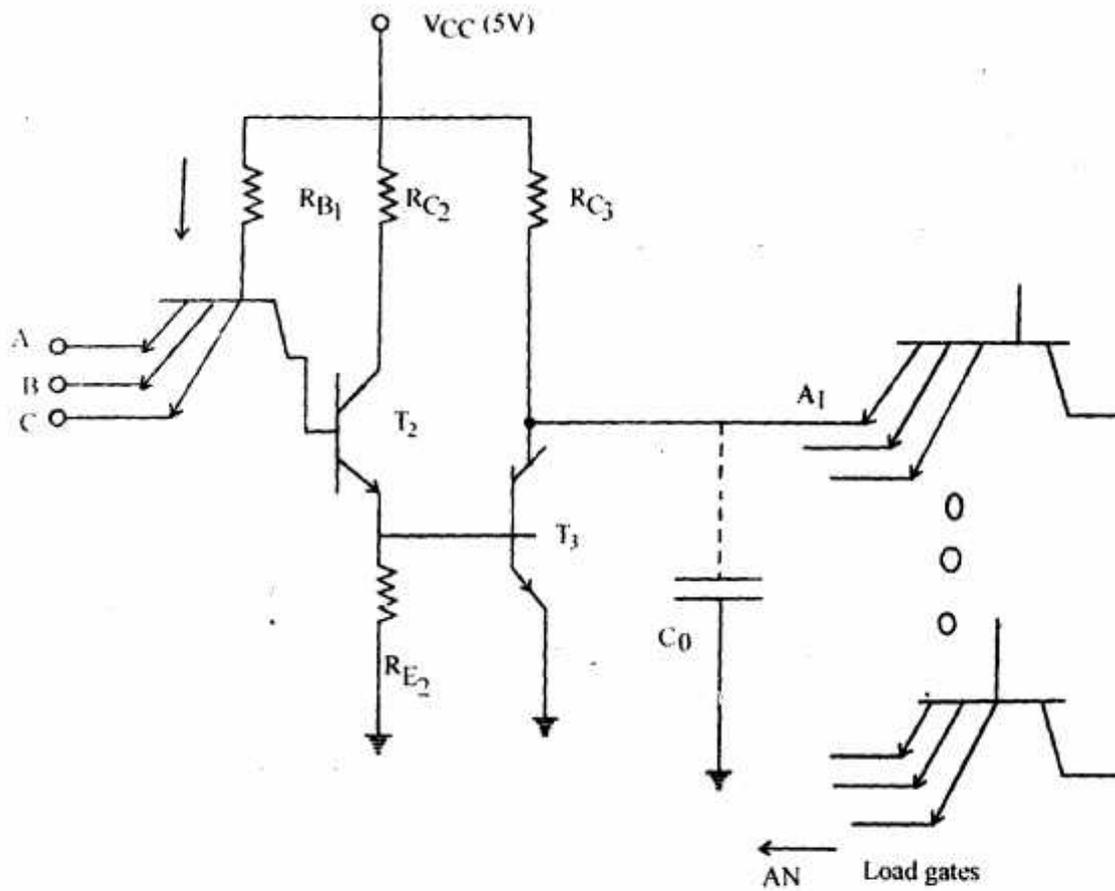
A three input TTL NAND gate driving N similar gates