# B.E.

Seventh Semester Examination, May-2009
Advanced Computer Architecture (CSE-401-E)

Note : Attempt any *FIVE* questions. All questions carry equal marks.

Q. 1. What do you mean by orthogonal instruction set? Explain the following instruction set architectures :

(i)   **Load/Store**   (ii)   **Register Memory**   (iii)   **Register Plug Memory.**
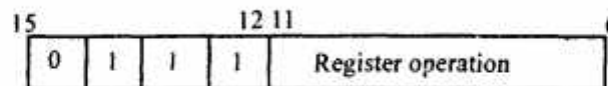
Ans. Basic Computer Instruction Frames :

15	14	12 11	0
0	Opcode	Address	
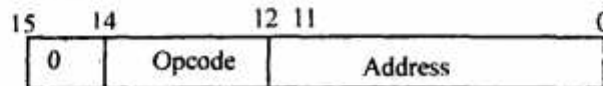
Opcode = 000 through 110
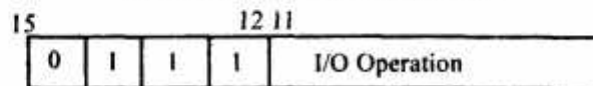
Member reference instruction

Register memory is the part of process common, better either on the processor chip or on the processor board. Register assignment is often made by the compiler.

15			12 11	0
0	1	1	1	Register operation

Opcode = 111

I = 0

(b) Register-Reference Instruction

15			12 11	
0	1	1	1	I/O Operation

Opcode = 111

I = 1

I/O Instruction

Register Plug Memory : Here transfer operations are directly controlled by the processor after instructions are decoded. Register transfer is conducted at processor speed, usually in one clock cycle.

Q. 2. (a) Compute the area in rbe with and without aspect-mismatch adjustment of a 32 kB direct mapped cache with 256-bit lines and a 20 bit tag.

Ans. Hexadecimal :

Address	Page number
60000	Page 0
60100	Page 1
60200	Page 2
60300	Page 3
60400	Page 4
604FF	Page 5

(a) Logical address assignment

Segment	Page	Block
6	00	012
6	01	000
6	02	019
6	03	053
6	04	A61

(b) Segment page vs mem., block assignment

Q. 2. (b) Write and explain the processor development life-cycle.

Ans.
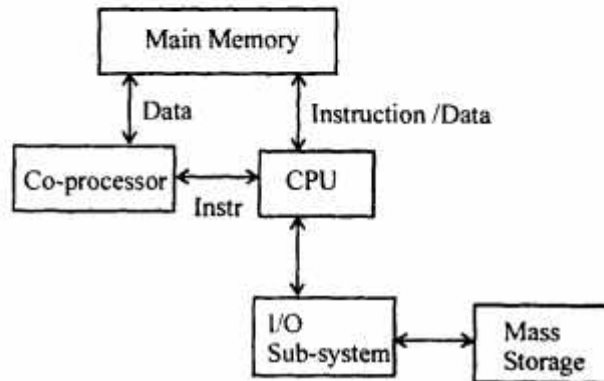
$$T = I_C \times (p + m \times k) \times e$$

The execution of an instruction requires going through a cycle of events involving the instruction fetch, decode & operand fetch, execution & store results.

In this cycle, only the instruction decode & execution phases are carried out in the CPU the remaining three operation's may be required to access the memory.

$$\text{MIPS Rate} = \frac{I_C}{T \times 10^6}$$

$$= \frac{f}{CPI \times 10^6}$$
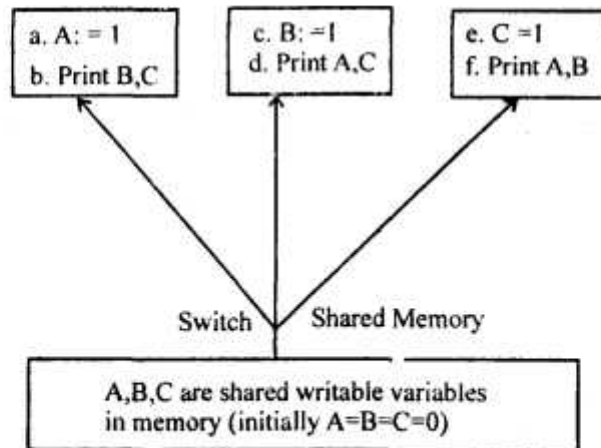
$$= \frac{f \times I_C}{C \times 10^6}$$

Throughput rate $\quad W_P = \dfrac{f}{I_C \times CPI}$ **Ans.**

Q. 3. A 128 kB cache has 64 B lines, 8 B physical word, 4K byte pages and is from way set-associative. It uses copy back and LRU replacement. The processor creates 30-bit (byte-addressed) virtual addresses that are translated into 24-bit (byte-addressed) real byte addresses. (Labeled –A_0......... A_{23}) from least to most significant.

(a) Show a complete layout of cache.

(b) Which addresses bits are unaffected by translation?

(c) Which address bits are compared to enteries in cache directory?

(d) Which address bits are used to address the cache directories?

(e) Which address bits are appended to address bits in (d) to address the cache array?

Ans.

Page Trace	7	24	7	15	24	24	8	1
working	7	7	7	7	8	8	8	8
set		24	24	24	9	9	9	1
			15	15	15	1	24	24

a. A: = 1	c. B: = 1	e. C = 1
b. Print B,C	d. Print A,C	f. Print A,B

Switch   Shared Memory

A,B,C are shared writable variables in memory (initially A=B=C=0)

Q. 4. Suppose two processors (in a multiprocessor system) make a total of exactly two references to memory every memory cycle (Tc = 100 ns) the memory consists of eight low order interleaved memory modules with Tacers = 120 ns. Find :

(a) Expected waiting time.

(b) Total access time.

(c) Mean total number of queued requests.

(d) Offered memory band width (references/sec)

(e) Achieved-memory band width using streeker's model.

Ans.
$$\pi = \int_0^1 f(x)\,dx$$

$$= \int_0^1 \frac{y}{1+x^2}\,dx = h\sum_{i=1}^{n} f(x_i)$$

Host program
Input(n)
send (n, all modes)

Node Program
p = num nodes( )
me = mynode( )

recv $\left(P_1^2\right)$

output (P_1)

secv (n)

h = 1.0/n

sum = 0

Do P = me + 1, n, p

$x = h \times (i - 0.5)$

sum = sum + f(x)

End Do

pi = hx sum

gap ('+', pi) host).

Q. 5. (a) What are the factors which affect the performance of a vector processor?

Ans. A solution is a set of scalar data item, all of the same type, stored in memory. Usually, the vector elements are ordered to have a fixed addressing increment between successive elements called the stride.

A vector processor is an ensemble of hardware resources including section registers, functional pipelines, processing elements & register counters for performing vector operations.

Depending on the speed sand between vector & scalar operations & on the vectorization ratio in user program, a vector processor executing a well vectorized code can easily achieve a speed up of 10 to 20 times as compared with scalar processing on conventional machines.

Relative vector/scalar performance :

$$P = \frac{1}{(1-f)+f/r} = \frac{r}{(1-f)r+f}$$

- Maintaining a good vector/scalar performance balance.
- Supporting scalability with an increasing number of processors.
- Increasing memory system capacity & performance.
- Providing high performance I/O & are easy access network.

Q. 5. (b) Explain briefly. How multiple issue machines are different from vectored machines?

Ans. In are is issue processors the instruction decoding & execution resources are increased to form essentially on pipelines operating concurrently.

The resource shared multiple pipeline structure is called superscaler processor.

Here, the processor can issue 2 instructions per cycle if there is no resource conflict & no data dependence problem.

In multiple issue machines, it is difficult to schedule multiple pipelines simultaneously, especially when the instructions are retrieved from the same source. Pipeline stalling should be avoided & pipeline idle time should be minimized.

Q. 6. (a) A far porterl (three read, one write) memory system would support a vector processor with what maximum speed-up over a uniprocessor? Explain.

Ans. Primitive memory operations for multiprocessors include load (read), store (write) and one more synchronous operations such as swap (atomic load-store) or conditional store. For simplicity, one representative synchronization operation swap, besides the load & store operations.

Conventional uniprocessor computers have been modeled as random access machines (RAM) by strength

& strings (1963). A parallel random access machine (PRAM) model has been developed by fortune & Wyeil (1978). For modeling idealized parallel computers with zero synchronous or memory access overhead.

PRAM Model
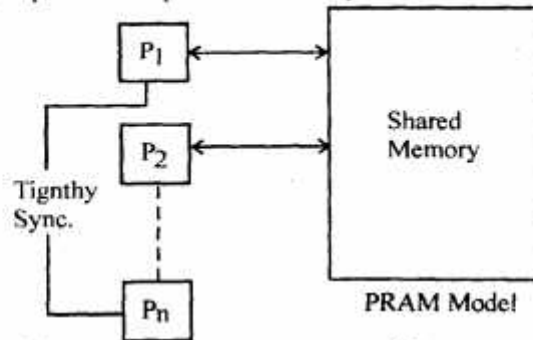
Exclusive Read (ER) : Allows or most one processor to read from any memory location in each cycle; a rather restrictive policy.
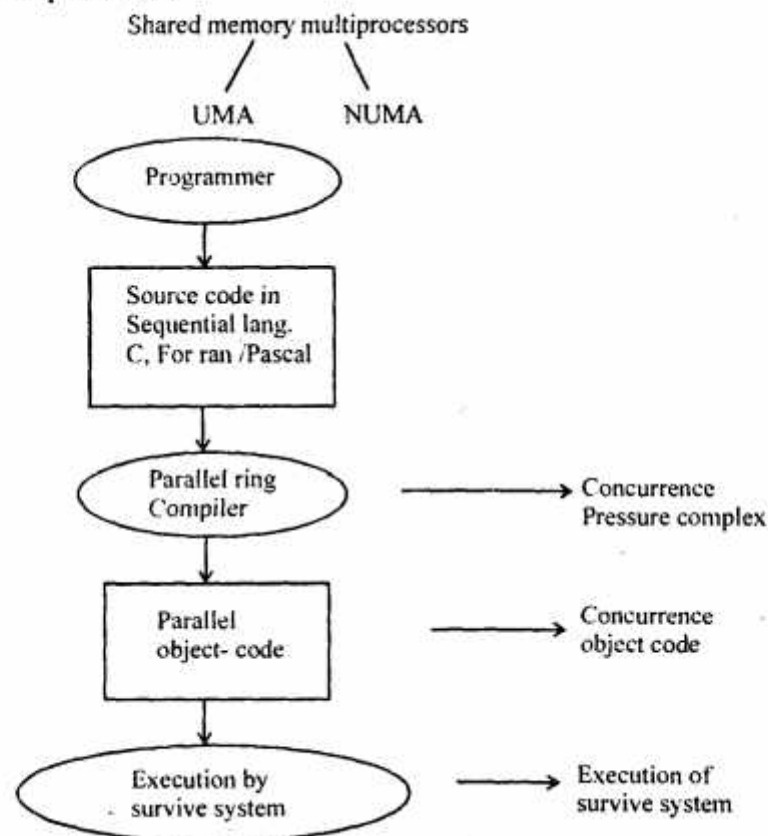
Exclusive (EW) Write : Allows or most one processor to write into a memory locations an a time.

To reduce the number of PEs to $n^3 / \log n$, use a PE array of size $n \times n \times n / \log n$.

Each PE is responsible for computing log n product terms & summing them up.

Q. 6. (b) Discuss the relative advantages of update and invalidate protocols for multi core switched shared memory multiprocessors.
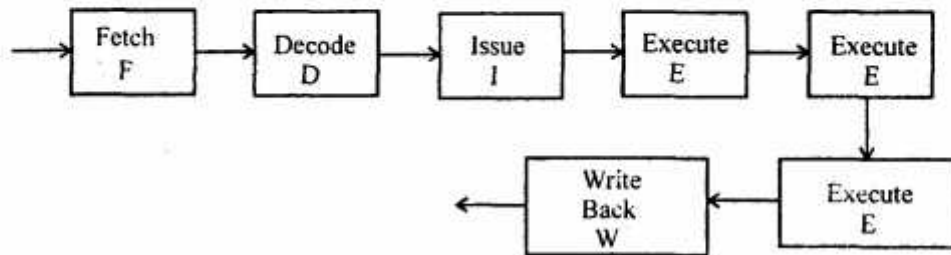
Ans.

Advantages :

- Full control
- Complex data & control structures are easily implemented.
- High throughput.
- Free from side effects.
- Very high potential for parallism.
- Only required instructions are executed.
- High degree of parallism.
- Ease manipulation of data structures.

Q. 7. (a) Write and explain the instruction execution cycle followed by a typical processor?

Ans.

(a) A seven stage instruction pipeline.

$$R_1 \leftarrow \text{Mem}(M)$$

$$R_2 \leftarrow \text{Mem}(Z)$$

$$R_3 \leftarrow (R_1) + (R_2)$$

$$\text{Mem}(x) \leftarrow (R_3)$$

$$R_4 \leftarrow \text{Mem}(B)$$

$$R_5 \leftarrow \text{Mem}(C)$$

$$R_6 \leftarrow (R_4) * (R_5)$$

$$\text{Mem}(A) \leftarrow R(6)$$

(b) In order instruction issuing

IF	IS	RE	EX	DF	DS	TC	WB			
	IF	IS	RF	EX	DF	DS	TC	WB		
		IF	IS	RF	EX	DF	DS	TC	WB	
			IF	IS	RF	EX	DF	DS	TC

(c) R4000 instruction overlapping in pipeline

Phase Including :

Fetch

Decode

Operational fetch

Execute &

Write back

The instructions are executed in are or several execute Srages (E). There execute stages are shown in fig. The loss write back stage (W) is used to write results into the registers.

Q. 7. (b) What are the problems encountered in the implementation of a pipelined processor.

Ans.

1. As the degree of super pipelining increases, the speedup curves show steady increases. The improvement of pipeline performance is similar. When the instruction issue rate increases in the plots.

2. The superscalar degree m is limited by the small I/P encountered in programs.

3. The pipeline clock cycle is limited by the multiphase clocking technology available for distributing clock phases and by the long setup time of registers.

4. The pipelined machine has a longer start up delay & lags behind the superscalar machine are the stress of program.

5. A branch may create more damage on the superpipelined machine than on superscalar machine.

Q. 8. (a) What do you mean by write assembly cache? How it is useful?

Ans. Caches can be addressed using either a physical address or a virtual address.

Data is written through the main memory immediately via a write through (WT) caches or delayed until block replacement by using a write back (WB) cache. A WT cache, requires more bus or network cycles to access the main memory, while a WB cache allows the CPU to continue without waiting for the memory to cycle.
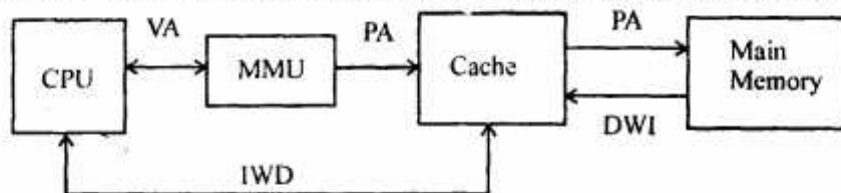
Usefulness :

– Include no need to perform cache flushing.

– No alining problems.

– Thus, fewer cache bugs in OS kernels.

Q. 8. (b) What are the design issues for multiprocessor systems? Explain.

Ans. SM = Shared Memory

LM = Local memory

P = Processor

C = Cache

Design Issue :

- Network control strategy is classified as centralized a distributed.
- Buses implemented on printed circular bands are called local buses.
- The architecture combines features from UMA, NUMA & COMA models.
- The processors share the access of I/O & peripheral devices through a processor I/O network (PIDN).
- Dynamic networks are used in multiprocessors in which the interconnections are under program control.

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