B.E.

Seventh Semester Examination, December-2008

Advanced Computer Architecture (CSE-401-E)

Note : Attempt any five questions.

Q. 1. (a) Discuss the advantages & disadvantages of using microprogrammed instruction decode.

Ans.

Attribute	Microprogrammed Decoders
Speed	slower
Chip area/efficiency	uses more area
Case of change, additions	easier
Ability to handle large	easier
Complex instruction sets ability to support	easy
Operating systems & diagnostic features where used	mainframes, some microprocessors
Instruction set size	usually over 100 instructions
ROM size	2^K-2^K by 40-200 bit microinstructions

Q. 1. (b) The roots of a quadratic equation are

$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

Write assembly code for finding roots for Load/Store architecture. Initial values of a, b, c are stored in Addr(R_1), Bddr(R_1), Cddr(R_1), where R_1 contains a base value that must be loaded. Assume a square root instruction SQRT.

Ans.

ACBF	F	(32 floating point)
ACBD	D	(64 floating point)
ACBG	G	(64 special floating point format)
ACBH	H	(128 special floating point format)
ADAWI		
ADDB1	add B	-2 add
		-3 add
ADDF2	add F	-2 add
ADDF3		-3 add
ADDG2	add G	-2 add
ADDG3		-3 add
ADDH2	add H	-2 add
ADDH3		-3 add
ADDL2	addL	-2 add
ADDL3		3 add
ADDD2	add D	-2 add

ADDD3		-3 add
ADDP4	add	packed 4 byte operand
ADDP4	add	packed 6 byte operand

Q. 2. A certain pipe line has the following functions & function unit delays without clocking overhead.

Function units *B, D, E* can be divided into two equal stages. If the expected occurrence of pipeline breaks is b = 0·25 and clocking overhead is 2 ns (K = 0) :

Function	Delay
A	6
B	8
C	3
D	7
E	9
F	5

(a) Ignoring quantization, what is the optimum number of pipeline segments (round to integer).

(b) What cycle time (with quantization) does this give ?

(c) Compute the performance of pipeline with this cycle time.

(d) If there is an additional ±1ns uncontrolled clock skew in (b), what is adjusted cycle time.

Ans. (a) Occurance of Branch classes
Branch (*BC, BR. BCR. BRR*)
Loop Control (*BCT...*)
Procedure (*BAL, BALR*)

(b) Branch :
Target address in register
Target address formed by *AG*

(c) Unconditional (*BR* and *BRR*)
Conditional - went to target
Conditional - went in-line

(d) Loop constructs
That go to target
That go in line.

Q. 3. (a) State and explain the principle of locality of reference. What are various types of localities.

Ans. The local miss rate of a second level cache is quite dependent upon the behaviour of the level one cache.

So long as the level 2 cache is the same as or larger than the level 1 cache, analysis by the principle of inclusion provides an excellent estimate of the behaviour of the level 2 cache.

The level 2 cache, so long as it is significantly larger than the level one cache is completely independent of level 1 cache's parameters.

Q. 3. (b) Discuss any 2 line replacement strategies at miss time with their probable advantages and disadvantages.

Ans. Line Replacement : The replacement policy determines which line to replace when a miss occurs and the cache is full. There are three replacement policies that have been widely discussed :

(i) Least Recently Used (LRU) : Under this policy, the line that was learn recently accessed would be the candidate for replacement.

(ii) First In First Out (FIFO) : Under this policy, the line that had been in the cache the longest is designated the line to be replaced.

(iii) Random Replacement (RAND) : Under this policy, replacement is determined randomly.

Q. 4. Derive the match logic for one word of cache memory (associative). Draw & explain the structure of associatively mapped cache memory.

Ans. ADD. F. *R*4, 8 [*R*3, *R*1]

I Fetch

PC → TLB

cache → SR

SR → IR

Decode

address generate

Data fetch

cache → SR

execute *R*4 + *SR* → *R*4

Next instr prep *PC* + 4 → *PC*

ST.F 0[*R*3, *R*4], *R*4

I fetch

PC → TLB

sache → SR

SR → IR

Decode

address generate

Data store

R4 → SR

SR → cache

Next instr prep PC + 4 → PC

Q. 5. In a two level cache system we have * L_1 size 8 kB with 4 w. set associative 16 B lines and wTNwA and *L_2 size 64 kB direct mapping 64 B lines and CB wA. suppose the miss in L_1, hit in L_2 delay is 3 cycles and the miss in L_1, miss in L_2 delay is 10 cycles. the processor makes 1.5 references/Instruction.

(a) What are L_1 and L_2 miss rates.

(b) What is expected CPI loss due to cache misses.

(c) Will all lines in L_1 always reside in L_2? Why ?

Ans.

Architecture Class	Architecure	Size
Reference	H'r machine	1·00
Stock	P code	10·12
R/M	S/370	6·23
R + M	VAX MAX	6·40

Architecture	L/S	R/M	R + M
Instruction fetched	1·98	1·78	1·14
I Bytes fetched	7·92	6·3	—

Simple			Reads	Writes
R/M	S/370	Fortran Hopv I	0·53	0·89
R + M	VAX UNIX	Fortran	1·11	1·66

Q. 6. Discuss the following memory models :

(a) Strecker's model

(b) Simple closed binomial model

Ans. This model assumes that there are n simple processor requests made per memory cycle & there are m memory schedules'. Further, we assume that there is no bus contention.

Modelling Approximations :

A processor issues a requests as soon as its previous requests has been satisfied.

The memory requests pattern from each processor is assumed to be uniformly distributed *i.e.*, the probability of any one request being made to a particular memory module is Y_m.

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$$B(m, n) = K\,[1 - (1 - Y_k)^r\,]$$

(b) Simple Closed Binomial Model : Suppose n is equal to 1. For a simple processor memory configuration, there is no memory contention & the achieved band width is $B(m, 1) = 1$

Now if $m = 1$ and $n > 1$, there is contention that but the achieved BW is the same $B\,(1, n) = 1$.

Suppose we had substitute the queue size for the $M_B/D/1$ (Binomail arrivals) for the M/D/1 as used in the developed of the asymptotic solution.

Now,

$$\mu = \frac{n}{m} = \rho_a + \frac{\rho_a{}^2 - p\rho_a}{2(1 - \rho_a)}$$

$$p = \frac{1}{m}$$

$$n/m = \rho = \rho_a + \frac{\rho_a^2 - \rho_a/m}{2(1-\rho_a)}$$

$$\rho_a = 1 + \frac{n}{m} - \frac{1}{2m} - \sqrt{(1+n/m-1/2m)^2 - 2n/m}$$

$$B(n,1) = x + 1 - \frac{1}{2} - \sqrt{\left[(x+1) - \frac{1}{2}\right]^2 - 2x}$$

$$= x + \frac{1}{2} - \sqrt{x^2 - x + 1/4}$$

$$= x + \frac{1}{2} - x + \frac{1}{2} = 1$$

Thus, the Binomial approximation is useful whenever we have :

(i) Simple processor memory configuration

(ii) $n \geq 1$ and $m \geq 1$

(iii) Request response behaviour between processor and memory where the processor makes exactly n requests per T_c.

Q. 7. (a) Compare and contrast the multiple issue machines and vector machines.

Ans. The alternative to vector processors is multiple issue machines. There are 2 broad classes of multiple issue machines : statically scheduled and dynamically scheduled.

Early static multiple issue machines include the so called VLIW machines. These machines use an instruction word that consists of 8 to 10 instruction fragments. Each fragments controls a designated execution unit, thus, the register set is extensively multiported to support simultaneous access to the multiplicity of execution multiported to support simultaneous access to the instruction word is typically over 200 bits long.

The issue of detection of independence within or among instructions is theoretically the same regardless of whether the detection process is done statically or dynamically.

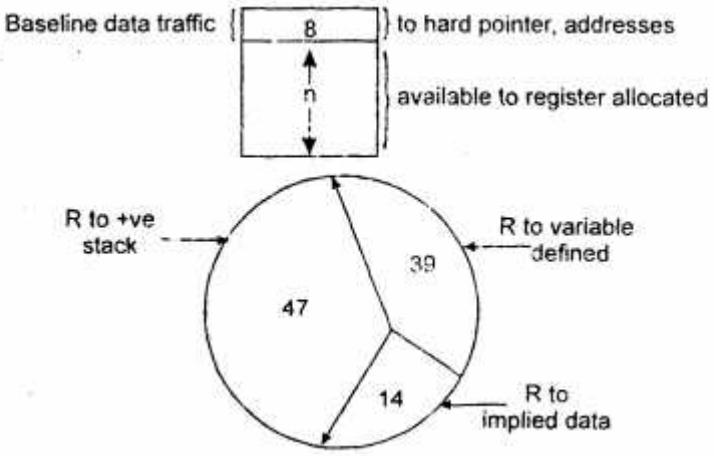
Q. 7. (b) A four ported (three read, one write) memory system would support a vector processor with what maximum speed-up over a uniprocessor. Explain.

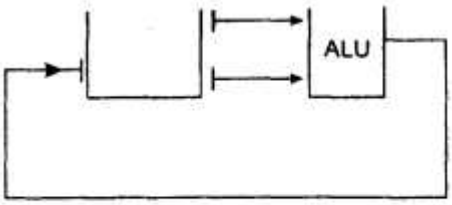
Ans. Registers may be organized in many different ways :

(i) As a conventional single register set

(ii) As multiple or windowed register sets

(iii) As a stack cache buffer or a contour buffer.





Multiported registers, registers can access 2 values & return a result within a single cycle.

Q. 8. Discuss the relative advantages and disadvantages of update and invalidate protocols for multinode switched shared memory multiprocessor.

Ans. Snoopy protocols can be categorised not only by whether they invalidate or update shared data line lines in remote caches, but also by the source of the new data for a cache line. The data may be provided either by the main memory or by the cache that makes the most receive write to the share data line.

Name	Category	Mem. copy policy
Invalidate	or invalid	copyback
Berkeley	or invalid	copyback
Illionious	or invalid	copyback
Firetly	or update	copyback
Dragon	or update	copyback