B.Tech.

Fifth Semester Examination

Microprocessors & Interfacing (EE-309-F)

Q. 1. (a) How many interrupts are maskable in 8085 microprocessor ?

Ans. In 8085 microprocessor four interrupts are maskable (RST 7.5, RST 6.5, RST 5.5 and INTR).

Q. 1. (b) Which signal of 8085 microprocessor is used to insert wait states ?

Ans. Ready is used by microprocessor to sence whether a peripheral device is ready for data transfer or not. If not the processor waits for synchronise with (slow) peripherals.

Q. 1. (c) Explain in brief about data bus buffer in 8253.

Ans. This tristate, bidirectional, 8 bit buffer is used to interface the 8253/54 to the system data bus.

Q. 1. (d) Why DMA facilities are required in microprocessor-based system ?

Ans. The DMA data transfer will be useful to transfer large amount of data between memory and input/output device in a short time.

Q. 1. (e) Why is the z-flag of a 8085 microprocessor not affected after execution of instruction MOV D, B ?

Ans. In 8085 microprocessor, zero flag is used to indicate the result of arithmetic or logic operation of ALU zero or non-zero for reset Z flag is zero and for set zero flag is 1.

Q. 1. (f) Which bit of the caught bit carry flag is affected when during the execution of an arithmetic operation, there is a carry of bit 3 to bit 4 ?

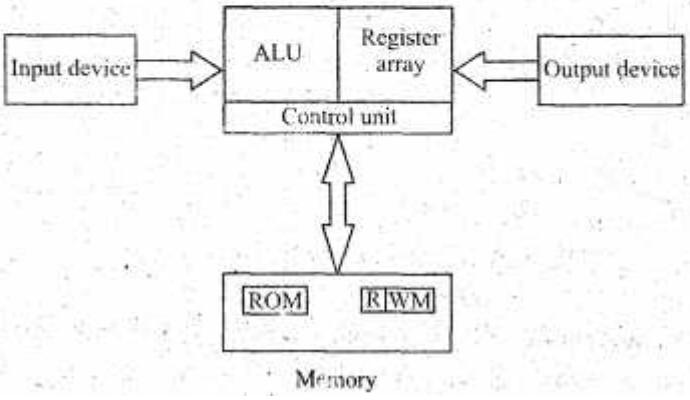
Ans. When a 8085 microprocessor, carry flag is generated from bit (D_3) pass on through bit 3 (D_3) pass through bit 4 (D_4) than auxiliary carry flag is set.

Q. 1. (g) In 8085 microprocessor based system how many maximum no. Memory and I/O device that can addresses ?

Ans. In 8085 microprocessor, we are using 8 bit address for I/O device and 16 bit address for memory.

Q. 1. (h) Draw block diagram of microcomputers.

Ans.



Q. 1. (i) Describe about Accumulator (A).

Ans. (i) It 8 bit S.P.R. and user accessible.

(ii) It acts as one source of operand to the ALU.

(iii) During I/O data transfer, data is transfer between accumulator (A) and I/O device.

Q. 1. (j) What is temporary register ?

Ans. Temporary Register : (i) It is a 8 bit S.P.R. which is not a user accessibly register.

(ii) It acts as end source of operand during ALU operation.

Section—A

Q. 2. (a) Compare between memory mapped I/O and Peripheral mapped I/O.

Ans.

Memory-mapped I/O	**Peripheral I/O**
16 bit	8 bit
$\overline{MEMR}$ $\overline{MEMW}$	$\overline{IOR}$ $\overline{IOW}$
Between any resister and I/O	Only between I/O and the accumulator
13 T-states (STA, LDA)	10-T-states
7-T-States (MOV MR)	
More Hardware is needed	Less Hardware is needed

Q. 2. (b) The following 8085 instruction are executed as :

XRA A
MOV L, A
MOV H, L
IUX H
DAD H

After execution of program of content find HL pair ?

Ans. We know that XRA A is the instruction through which we clear the accumulator.

So, after XRA A

We get [A] ← 00H

Again [L] ← 00H

After IN× H

We get [HL] ← [HL]+0001H

Again DAD H means

$$[HL] \leftarrow [HL]+[H]=0001H+001H$$

∴ Content of HL pair = 0002H

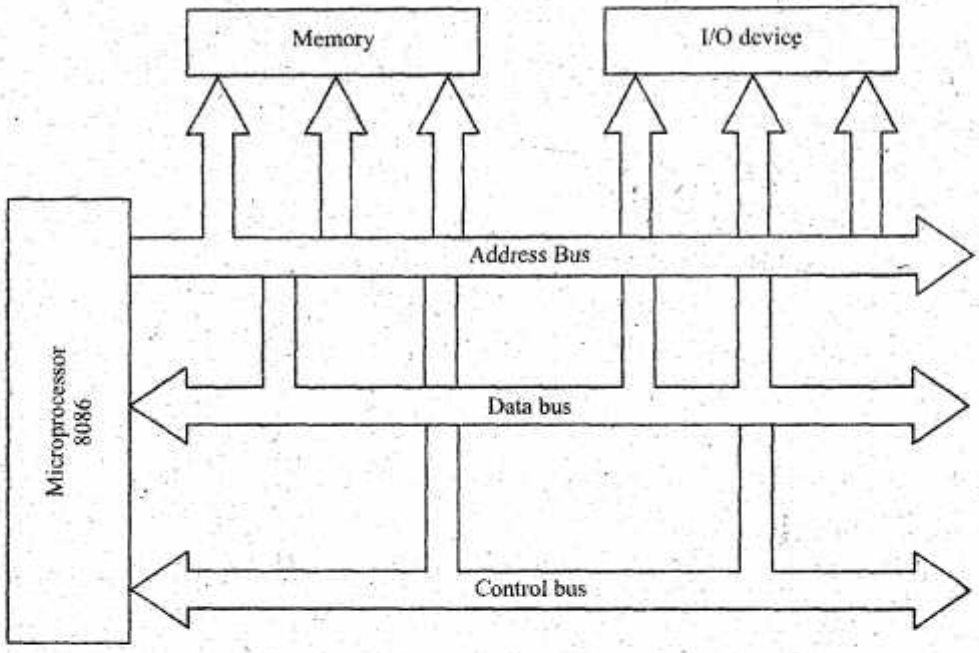
Q. 3. Describe memory and input/output interfacing in 8086 microprocessor.

Ans. (i) Several memory clips and I/O device are connected to a microprocessor.

(ii) Figure below show interface memory clips or I/O device of microprocessor.

(iii) If IO/$\overline{M}$ is high the decoder 2 is activated and required I/O device is selected.

(iv) If IO/$\overline{M}$ is low the decoder is activated.



Section—B

Q. 4. Consider an 8085 microprocessor system the following program starts at location 0100H

LXI SP, 00FF
LXI H, 0107
MVI, 20H
SUB M

What is contain of accumulator when program counter reaches 0109H.

Ans. 0100 LXI SP, 00FF
0103 LXI H, 0107
0106 MVI A, 20 H
0108 SUB M → A ← A — M
0109

M contains the data of memory whose address which is in HL pair. HL has address 0107.

0107 corresponds to 20H

∴ A-M = 20H – 20H = 00H

Q. 5. (a) If in addition following code exists from 0109H onwards.

ORI 40 H

ADD M

What will be the result in accumulator after the last instruction is executed ?

Ans. 0109H ORI 40H

0108 H ADD M

A ← 00H = 00000000

40H = 01000000

ORI → 01000000

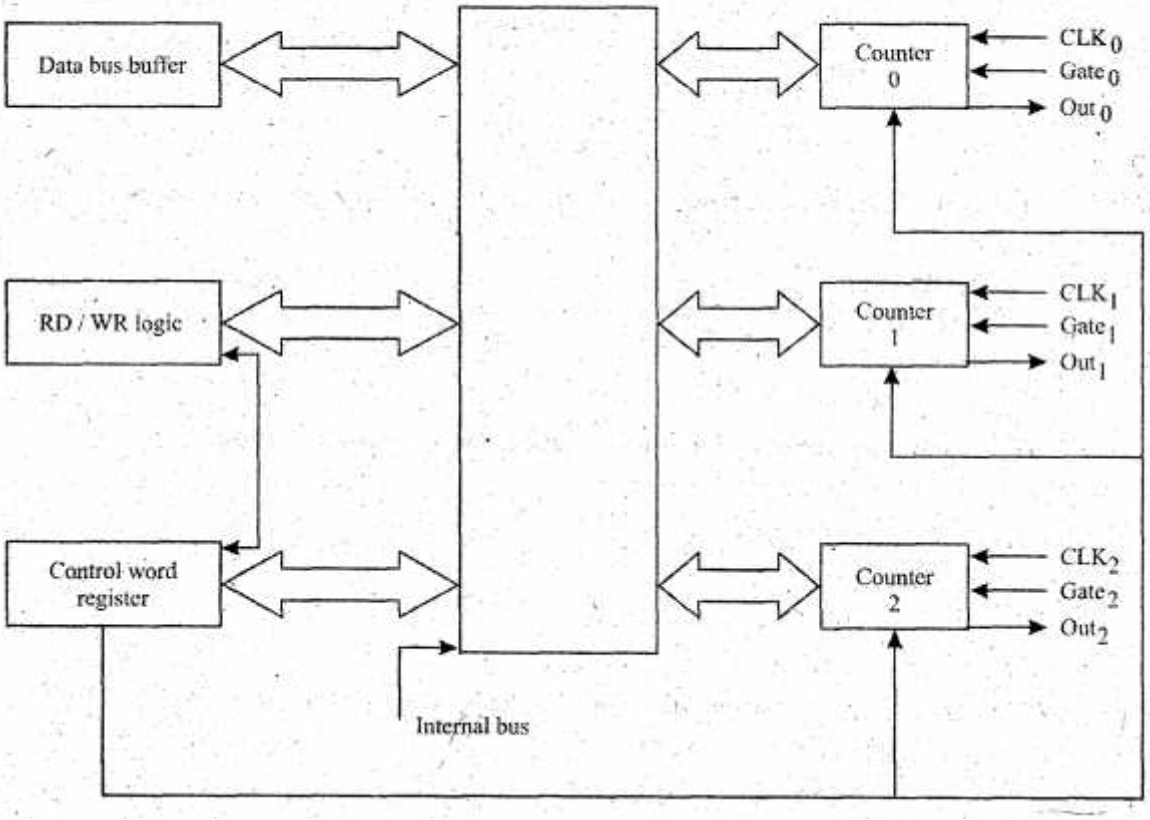
A → 40H

A ← A + M = 40H + 20H

A ← 60H

Q. 5. (b) Draw block diagram of a programmable internal timer (8254).

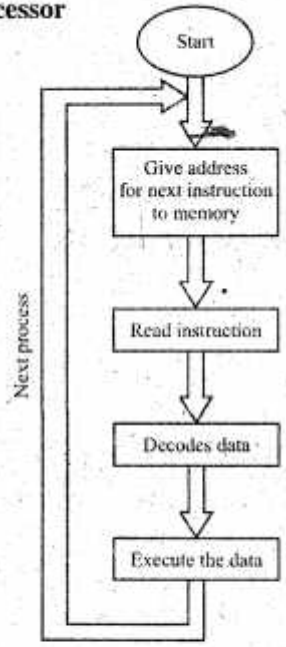
Ans. Block diagram of 8254 :



Section—C

Q. 6. Describe flow chart of microprocessor. Also explain system bus.

Ans. Flow Chart of Microprocessor



Microprocessor basically contains four parts :

(i) Central processing unit (C.P.U.)

(ii) Memory i.e., RAM, ROM, R/WM

(iii) Input device, i.e., keyboard, scanner, mouse etc.

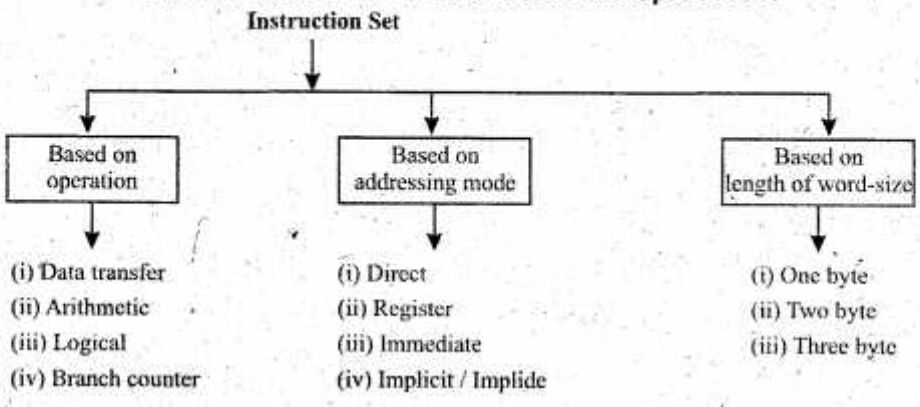
(iv) Output device, i.e., printer, speaker, monitor.

System Bus : It is a communicational path between microprocessor and peripherals.

Q. 7. (a) What do you understand by instruction set ? Classified instruction set.

Ans. Instruction Set : It is connection of instruction of microprocessor, that determine what function that microprocessor can perform.

Classification of Instruction Set in Microprocessor



Q. 7. (b) Explain data bus buffer of 8253.

Ans. Data Bus Buffer of 8253 : This tri-state, bidirectional, 8 bit buffer is used to interface the 8253/8254 to the system of data bus.

Functions :

(i) Programming of 8253/8254 in various mode.

(ii) Loading the counter register.

(iii) Reading the count values.

Section—D

Q. 8. An 8085 execute the following instructions as

MVI A, 89

MVI B, 74

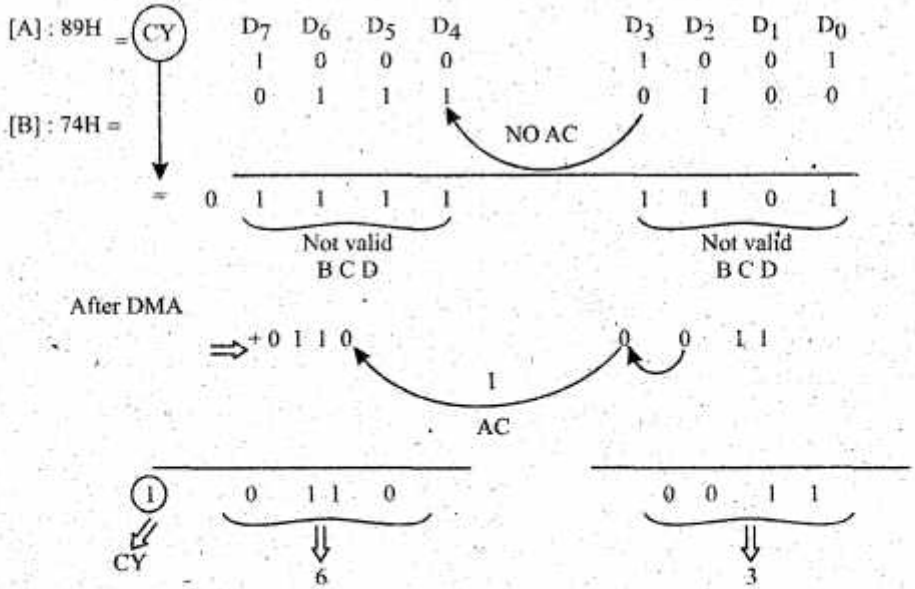
ADD B

DAA

Evaluate the content of accumulator and status of flags are.

Ans. MVI A, 89 means data, "89" should move immediate into 'A'.

After ADD B instruction, we get



Flag status are

AC = 1, CY = 1, P = 1, Z = 0, S = 0

Accumulator contain ⇒ [A] ← [63H]

Q. 9. (a) Describe about arithmetic group of instruction set.

Ans. In this group the data is perform as addition, subtraction, increment (add 1), decrement (subtract I) etc.

(i) Important is the arithmetic group of operation implicitly assumed that the contents of the accumulator are one of perfect previous contain of accumulator remain unaltered.

(ii) The result of arithmetic operation result in accumulator.

(iii) The flag are modified to reflect the data condition of operation.

(iv) The contents of register are not change as a result of arithmetic operation.

Q. 9. (b) Explain read/write logic of 8253/8254.

Ans. The read/write logic register have five signal $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ and address line A_0 and A_1. In the peripheral I/O mode a $\overline{RD}$ and $\overline{WR}$ signals are connected to $\overline{IOR}$ and $\overline{IOW}$ respectively :

A_0	A_1	Section
0	0	Counter-0
0	1	Counter-1
1	0	Counter-2
1	1	Control word register