B.E.

Fifth Semester Examination, December-2008

Microprocessor & Interfacing (EE-309-E)

Note : Attempt any five questions. All questions carry equal marks.

Q. 1. (a) Describe the purpse of following in 8085 :

(i) Program counter **(ii) Stack Pointer** **(iii) Accumulator ALU and Flags**

(iv) Serial I/O Control **(v) Instruction Register**

Ans. (i) Program Counter : This is 16 bit register deals with the four operations, sequencing the execution of instructions. This register is a memory pointer. Memory locations have 16 bit addresses and that is why this is a 16 bit register.

(ii) Stack Pointer : Stack pointer is also a 16 bit register used as a memory pointer, initially it will be called the stack pointer register to emphasive that it is a register.

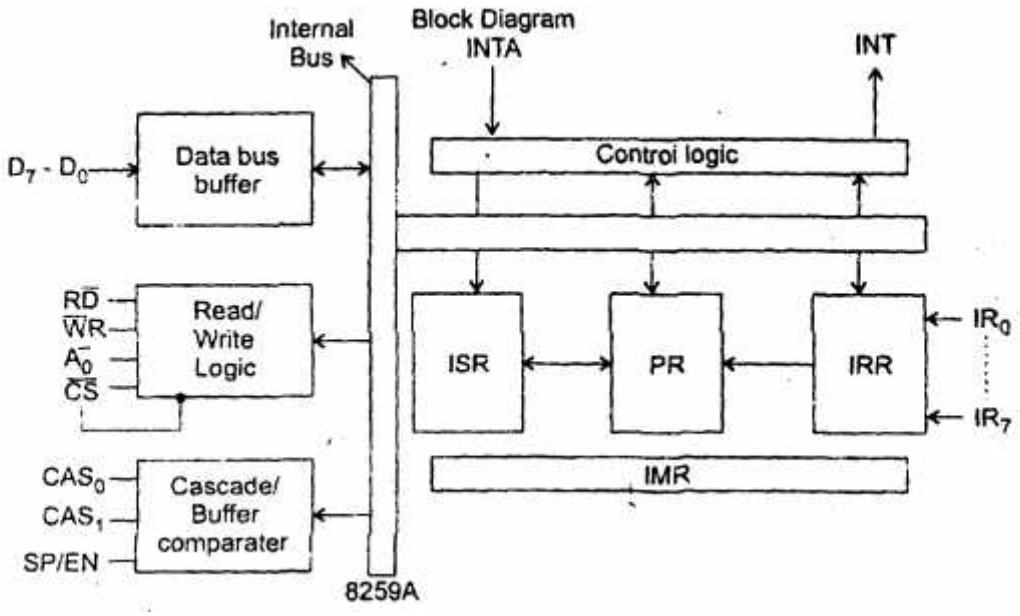
(iii) Accumulator ALU and Flags : The accumulator is an 8 bit register that is part of the ALU register is used to store 8 bit data and to perform arithmetic and logical operations.

(iv) Serial I/O Control Requirement : The microprocessor identifies the peripheral through a poor address and enables it using the read or write control signal to interface program control or interrupt control.

(v) Instruction Register : 8085 has 6 general purpose registers to perform the first operation. These registers are identified as B, C, D, E, H, L.

Q. 1. (b) Describe the working of interrupt I/O control in 8085.

Ans.



Q. 2. (a) Write a program in Assembly language of 8085 to set sign flag, zero flag. parity flag and reset auxiliary carry and carry flag using stack operation.

Ans.

```
DCR  D
EI
RNZ

DI
MVI D, 3CH

MOV A, C
ADD 01H
DAA
MOV C, A
CPI. 60H
EI
RNZ

DI
MVI C, 00H
INR B
RET
```

Q. 2. (b) Describe various addressing modes of 8085 with suitable examples.

Ans. Memory Mapped Input/Output :

Memory add	Machine code	Mnemonics
2050	32	STA, 8000 H
2051	00	
2052	80	

Multi Port Addressing :

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	0	0	1	0	0	= 84 H
		0	1					= 8 CH
		1	0					= 94 H
		1	1					= 9 CH

Q. 3. (a) Describe the purpose BIU and EU in 8086.

Ans. BIU is divided into following units :

(i) Instruction queue

(ii) Segment registers

(i.i) Instruction pointer

(iv) Bus control and address generator.

Segment register	Memory Segment	Default offset register
CS	Code	IP
DS	DATA	All except IP, BP SP
SS	Stack	SP, BP
ES	Extra	All except IP, SP, BP

EU has following parts :

(i) Instruction Decoder & Control subsystem

(ii) ALU

(iii) Flag Register

(iv) General Purpose Register

(v) Index & Pointer Registers

ALU

ND	ND	ND	OF	DF	IF	SF	ZF	NF	AF	ND	PF	ND	CF

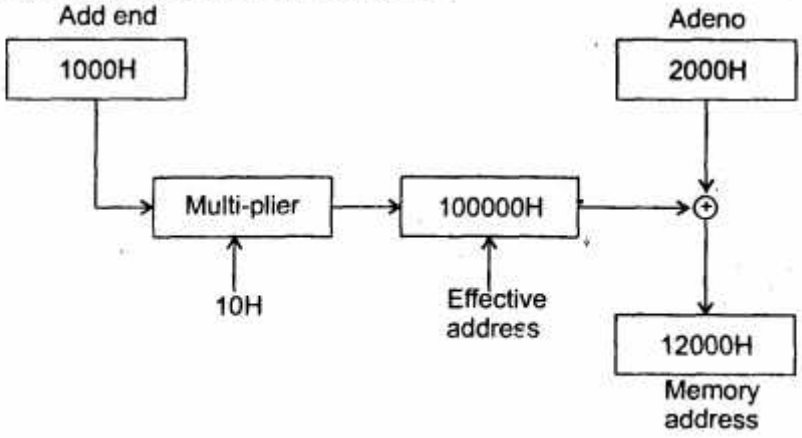
Carry Flag :

ADD FFFFh, AAA Ah

```
  F F F F
+ A A A A
---------
1 A A A 9
---------
↑ Carry
```

Q. 3. (b) Describe the purpose of segment and offset address in 8086. Compute physical address in DS = 46 A 9h and offset address in BX is 6A9Bh.

Ans.



CS	2	0	0	0	0	
IP		F	F	F	F	
	2	F	F	F	F	H

Q. 3. (c) What is program relocation ? How it is supported by segmented addressing ?

Ans. Segmented memory addressing on the other hand divides the memory into many segments. For example : The 1 MB memory is divided into smaller segments of 64kb. Each of these segments can be considered as a linear memory space as discussed.

Thus, if a segment registers has any arbitrary value XXXXH, the 8086 assumes it points to XXXX 0H. This is known as the segment base address. Efficiency this means that the segment register is used to reference to zeroth address of the segment.

SS	1	0	0	0	0	H	← BA
SP		A	B	B	C	H	← OA
	1	A	B	B	C	H	← PA

Segment addressing can be done by different Base addresses.

Q. 4. (a) Write a program in assembly language of 8086 which reads a character and

(i) Prints corresponding capital alphabet if it is small.

(ii) Prints corresponding small alphabet if it is capital.

(iii) Otherwise prints it as it is.

Ans. PAGE 60 , 120

```
0000
0000    0078        A       DW      120
0002    00E8        B       DW      232
0004    ????        C       DW      ?
                DATA SGENDS

0000    CODESGMAIN SEGMENT PARA 'CODE'
0000    PROGRAM PROC FAR

0000    BB_R MOV DS, DATASG

0003    A1 0000R MOV AX,A
0006    A30004 R MOV AX,A
000A    A30004 R MOV AX,B
0000    B8 170C  MOV C, AX

0010    CD  21  INT  21 H

0012    CODESGMAIN ENDP
        END PROGRAM
```

Q. 4. (b) Describe the purpose of following pins in 8085

(i) $\overline{BHE}$ and A_0 **(ii) NMI, INTR, $\overline{INTR}$**

(iii) $\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$ **(iv) $\overline{TEST}$**

Ans. EV can be broken down into

— Instruction decoder

— ALU

— Flag Register

— Index and Pointer Registers

8086 contains nine active flags which are of 2 types

— Conditional flags

— Control flags

CF — ZF

— CF

— SF CF — IF

— OF — DF

— ACF — IF

— PF

Q. 5. (a) Write the purpose of following assembly directives

(i) dosseg **(ii) db**

(iiii) dw **(iv) model**

Ans. Segment name SEGMENT PARA

STACK_SEG SEGMENT PARA STACK

Class Name	SEGMENT LINKED
'Code'	CODE SEGMENT
'data'	DATA SEGMENT
'stack'	STACK SEGMENT

Name	OPERATION	OPERAND
Code_seg	Segment	
Proc_one	Proc	
	⋮	
Proc_one	ENDP	Procedure ends
code_Seg	ENDS	

Q. 5. (b) Write the purpose of following instructions in 8086 :

(i) LOOP (ii) DIV (iii) CBW (iv) CWD (v) TEST

(vi) MOVSB (vii) Test (viii) SHR (ix) MOVSB (x) CMPSB

Ans. Instructions :

MOV AX, DX; 16 bit data transfer

MOV BX, AX; 16 bit data transfer

MOV AL, CH; 8 bit data transfer

MOV, Cr, Br; 8 bit data transfer

ADD AX, 16 bit data transfer

ADD AL, 8 bit data transfer

MOV mem/reg.

MOV, AL, CL

MOV AX, CX

DIX ram/reg.

DIV CX.

Q. 6. (a) Describe how 8285 can be configured using control register. Describe the purpose of various bits in control register.

Ans. The control section has five signals

— $\overline{RD}$

— $\overline{WR}$

— $\overline{CS}$

— Address lines A_0 and A_1

In the peripheral input/output mode, the $\overline{RD}$ and $\overline{WR}$ signals are connected to $\overline{IOR}$ and $\overline{IOW}$, respectively. In memory mapped input/output, these are connected to $\overline{MEMR}$ and $\overline{MEMW}$.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC-Select Counter :

SC1	SC0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Read Back Command

BCD	
0	Binary counter 16 bits
1	BCD counter (4 Decades)

Q. 6. (b) Describe the handshake signals for input/output port in 8085.

Ans. The MPV & peripherals operate at different speeds; therefore signals are exchanged prior to data transfer between the four responding MPV and slow responding peripherals such as printers and data convertors.

These signals form are called handshake signals. The exchange of handshake signals presents the MPV from writing over the previous data before a peripheral has had a chance to accept it or from reading the same data before a peripheral has had time to send the next data type.

Data input with handshake.

Similarities between Handshake Signals :

(i) Handshake signals ACK and STB are input signals to the device and perform similar functions, although they are called by different names.

(ii) Handshake signals DBF and IBF are output signals from the device and perform similar functions.

Q. 7. (a) Describe the DMA process and explain the working of 8237 DMA processor.

Ans. The direct memory access (DMA) is a process of communication or data transfer controlled by an external peripheral. In situations in which the microprocessor and controllers data transfer is to low, the DMA is generally used; data transfer between a floppy disk and R/W memory of the system. The 8085 µp has 2 pins available for this type and input/output communication :

— HOLD

— HLDA

HOLD : This is an active high input signal to the 8085 from another master requesting the use of address and data buses.

HLDA : Hold acknowledge, this is an active high output signal indicating that the MPV is relinquishing the control of the buses.

Q. 7. (b) Explain the working of 8259 programmable interrupt controller.

Ans. 8259A is a programmable interrupt managing device, specifically, designed for use with the interrupt signals (INTR|NT) of the 8085 µprocessor. The primary features of 8259A are as follows :

(i) It manages eight interrupt controls.

(ii) In can vector an interrupt request anywhere in the memory map through program control without additional hardware for restart instructions.

(iii) It can solve eight levels of interrupt priorities in a variety of modes.

(iv) With additional 8259A devices, the priority scheme can be expanded to 64 levels.

Implementing interrupts in the simplest format without cascading requires 2 specific instructions. After these instruction have been written, the following sequence of events shown occur :

(i) One or more interrupt request lines go high requesting the service.

(ii) The 8259A resolves the priorities and sends an INT signal to the MPV.

(iii) The MPV acknowledge the interrupt by sending $\overline{INTA}$.

(iv) After the $\overline{INTA}$ has been received, the opcode for the call instruction is placed on the data bus.

(v) Because of the CALL instruction, MPV sends 2 more $\overline{INTA}$ signals.

(vi) At the first $\overline{INTA}$, the 8259A places the low order 8 bit address on the data bus and at the second $\overline{INTA}$, it places the high order 8 bit address of the interrupt vector. This completes the 3 byte call instruction.

(vii) The program sequence of the MPV is transferred to the memory location specified by the CALL instruction.

Q. 8. Write short notes on following :

(a) Address/data multiplexing

(b) 8284 clock generator

(c) Trap, over flow and direction flag in 8086.

Ans.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M_2	M_1	M_0	BCD

SC-Select	Counter	
SC1	SC0	
0	0	Select counter 0
0	1	 1
1	0	 2
1	1	Read Back command

M-Mode

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
×	1	0	Mode 2
×	1	1	Mode 3

1	0	0	Mode 4
1	0	1	Mode 5

RW-Read/Write :

RW_1	RW_0	
0	0	Counter which command
0	1	R/W ISB only
1	0	R/W MSB only
1	1	R/W ISB first then MSB

BCD	
0	Binary counter 16 bits
1	BCD counter BCD 4 decades

Mode 8254 can operate in 6 different modes and the gate of counter is used either to disable or enable counting.