Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III • EXAMINATION – SUMMER 2013

Subject Code: 130704 **Date: 23-05-2013**

Subject Name: Computer Organization and Architecture

Time: 02.30 pm - 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define following terms 1. RTL 2.Micro-operation 3.Accumulator 4.Interrupt 5.Parallel processing 6.Assembler.	**6**
	(b)	Draw the block diagram of 4-bit arithmetic circuit and explain it in detail.	**8**
Q.2	**(a)**	Define Instruction Cycle. Explain its phases in brief with example.	**7**
	(b)	Explain the process of first pass of an assembler with flow chart.	**7**
		OR	
	(b)	Draw and explain flow chart of Interrupt Cycle.	**7**
Q.3	**(a)**	Write an assembly language program to subtract two double precision numbers.	**7**
	(b)	What is an addressing mode? List and explain various addressing modes of a computer with example.	**7**
		OR	
Q.3	**(a)**	Write an assembly language program to take a character as input and outputs it.	**7**
	(b)	What is the importance of status bits for program control? Which types of status bits are stored in a status register? Explain it with block diagram.	**7**
Q.4	**(a)**	Draw and explain block diagram of BCD adder.	**7**
	(b)	Explain Stack Organization of a computer system. Explain push and pop operations on register stack.	**7**
		OR	
Q.4	**(a)**	Explain the concept of overlapped register window for a procedure call.	**7**
	(b)	Differentiate memory reference and non-memory reference instructions. Give example of each with required micro-operations.	**7**
Q.5	**(a)**	Differentiate RISC and CISC.	**6**
	(b)	Attempt **any TWO**	**8**
	1	Pipelining technique.	
	2	Booth Multiplication Algorithm.	
	3	Memory Interleaving.	

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