Roll No. .....

24143

B. Tech (4th Semester) E.E./E.E.E./E.C.E. /E.I.E./I.C.E. Examination – May, 2012

DIGITAL ELECTRONICS

Paper : EE-204-F

Time : Three hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *one* question from each Unit. *Question No. 1 is compulsory.*

1. (a) What is Latch. 5 × 4

(b) Compare de-multiplexer with decoder.

(c) Design Ex-OR gate using NAND gate.

(d) Explain multiplexer.

UNIT – I

2. (a) Discuss error detecting and correcting codes. 10

(b) Subtract $(14)_{10}$ from$(7)_{10}$ by using 2's complement subtraction method. 10

3. (a) Simplify the given function using K-map $Y = \Pi\, m(0, 1, 2, 3, 5, 7, 14) + d(6, 9, 11, 12, 13, 15)$.10

(b) Minimize the function using Tabular method $Y = \sum m(0, 1, 3, 5, 7, 12, 13, 14, 15)$. 10

UNIT – II

4. (a) Explain cascading of two 1 : 4 demultiplexers to convert into 1 : 8 demultiplexer. 10

(b) Implement the full Adder with a decoder circuit. 10

5. Explain binary Adder and Subtractor. 20

UNIT – III

6. (a) Construct a D-flip flop using JK-flip flop. 10

(b) Design a synchronous binary MOD-6 counter. 10

7. (a) What is race around condition and how we can remove it. 10

(b) Explain Bidirectional shift register. 10

UNIT – IV

8. (a) Draw and explain the structure of PLA. 10

(b) Design the CKT for half adder using ROM. 10

9. Design Excess-3 to BCD code converter using PAL. 20
