Roll No. .....

2013

B. E. 3rd Semester (I.T.)

Examination – December, 2009

DIGITAL ELECTRONICS

Paper : EE-204-E

Time : Three hours] *[Maximum Marks : 100*

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Implement Boolean expression for EX-OR gate using NAND gates. 10

(b) Determine the single error correcting code for the BCD number 1001 using even parity. 10

2. (a) Simplify and design the given Boolean function using K-map

$y = \Sigma m (0, 4, 8, 12, 16, 18, 20, 22) + \Sigma d (24, 26, 28, 30, 31)$ 10

(b) Simplify the following Boolean function by using tabulation method.

$$F(A, B, C, D) = \Sigma m (0, 2, 3, 6, 7, 8, 10, 12, 13)$$ 10

3. (a) Implement the following Boolean function with 8 : 1 multiplexer.

$$F(A, B, C, D) = \pi m (0, 3, 5, 6, 8, 9, 10, 12, 14)$$ 10

(b) Design a full adder using 8 : 1 multiplexer Ic's. 10

4. (a) Convert the given D flip-flop to T flip-flop. 10

(b) Design MOD4 counter using JK flip-flops and implement it. 10

5. (a) Draw a TTL circuit with totem pole output and explain its working. Why should it not be used for wired AND connection ? 10

(b) Explain the working of ECL logic with suitable diagram. 10

6. (a) What are the specification of A/D converters ? Also explain the working of Dual-slope A/D converter with diagram. 10

(b) Explain sample and hold circuit with suitable diagram. 10

7. (a) What is tri state logic ? Where it is used ? 10

(b) Explain BCD subtractor with suitable diagram. 10

8. Write short notes on the following : $10 \times 2 = 20$

(i) ROM

(ii) CPLD