Roll No. .....

24165

B. Tech 4th Semester (Information Technology)

Examination – May, 2013

COMPUTER ARCHITECTURE AND ORGANISATIONS

Paper : CSE-210-F

Time : Three hours] *[Maximum Marks : 100*

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt ***five*** questions in all. Question No. 1 is ***compulsory*** and attempt ***one*** question from each Section.

1. (a) Describe De'Morgan's law. 8 x 2.5

(b) Differentiate between latch and a flip flop.

(c) Differentiate between logical shift and circular shift operation.

(d) Compare static and dynamic memory types.

(e) Define the terms : Seek time, Rotational Delay, Access time.

(f) Define the terms : locality of reference, cache hit, cache miss, hit ratio.

(g) Explain advantages of using a pipelining.

(h) Explain the format of microinstruction.

SECTION – A

2. (a) Design and explain the following : 14

(i) 2-bit full adder

(ii) J-K flip flop

(b) Explain MIPS and MFLOPS. 6

3. (a) Draw all logic gates from NAND gate. 7

(b) Write note on performance metrics. 7

(c) Explain multilevel view point of a machine. 6

SECTION – B

4. (a) Explain any five arithmetic and five shift instructions. 10

(b) Compare RISC architecture with CISE architecture. 10

5. Explain various Addressing modes by giving suitable example for each mode. 20

SECTION – C

6. (a) A digital computer has a memory unit of 64K * 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words :

(i) How many blocks can be cache accommodates ?

(ii) How many bits are there in the tag, index, block, and words field of the address format ?

(iii) How many bits are there in each word of cache, and how they are divided into functions ? 12

(b) Explain memory Hierarchy. 8

7. (a) Compare set-associative mapping with direct mapping. State the difference between a cache line and a cache block. 10

(b) What are the different types of semiconductor memories ? Give their merits and demerits. 10

SECTION – D

8. (a) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a 6 segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed that can be achieved ? 12

(b) Compare instruction level parallelism with processor level parallelism. 8

9. Write notes on the following : 20

(a) Control memory,

(b) Various types of interrupts,

(c) Stack organization.