

Roll No. ....

**24165**

**B. Tech 4th Sem. (Information  
Technology/C. E. E.)**

**Examination – May, 2012**

**COMPUTER ARCHITECTURE AND ORGANISATIONS**

**Paper : CSE - 210-F**

***Time : Three Hours ]***

***[ Maximum Marks : 100***

*Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complain in this regard, will be entertained after examination.*

**Note :** First question is *compulsory*. Attempt *five* questions in all selecting at least *one* question from each Unit. All questions carry equal marks.

**1. Write short notes on the following : 20**

- (a) Logic Gates
- (b) Latches
- (c) Addressing Mode
- (d) RAM
- (e) PROM

24165-8,200-(P-3)(Q-9)(12)

P. T. O.

- (f) Interrupt
- (g) Cache
- (h) Instruction Set

### UNIT - I

- 2. Describe Flynn's classifications of computers in detail with appropriate examples. 20
- 3. (a) Explain Instruction Set Architecture in detail. 10
- (b) Explain different types of instructions applied on instruction set with examples. 10

### UNIT - II

- 4. Define addressing modes ? Explain different types of it with examples. 20
- 5. (a) Design the microinstruction sequence counter. 10
- (b) Explain associative organization of cache memory. 10

### UNIT - III

- 6. Explain accumulated based CPU architecture types and solve the equation  $X = (A+B) * (C+D)$  using above said architecture. 20
- 7. A computer uses RAM chips of  $1024 \times 1$  capacities. Answer the following : 20

24165-8,200-(P-3)(Q-9)(12) (2)

- (a) How many chips are needed and how should there address lines be connected to provide a memory capacity of 1024 bytes.
- (b) How many chips are needed to provide a memory of 16 K bytes.

#### UNIT – IV

8. (a) Explain Amdah's law in detail. 10
- (b) Explain micro-processor level of parallelism. 10
9. (a) Explain types of instruction in 8086 in detail. 10
- (b) Design Binary to Octal decoder. 10