B.TECH.

[EEC-201]

SECOND SEMESTER THEORY EXAMINATION 2010-11

ELECTRONICS ENGINEERING

Time : 3 Hours   *Total Marks : 100*

Note: Attempt all questions.

1. Attempt all questions: (2×10=20)

Q.1. (a) If V_m is peak voltage across secondary of a transformer in a bridge full wave rectifier, then peak inverse voltage is given by:

(i) V_m (ii) $V_m/2$

(iii) $2V_m$ (iv) None of them

Ans. (iii) $2V_m$

Q.1. (b) The Avalanche breakdown in semiconductor diode occurs when:

(i) Forward current exceeds a certain value

(ii) Reverse bias exceeds a certain value

(iii) Forward bias exceeds a certain value

(iv) The potential barrier is reached to zero.

Ans. (ii) Reverse bias exceeds a certain value

Q.1. (c) A transistor is operating in active region, under this condition:

(i) both the junctions are forward bias

(ii) both the junctions are reverse bias

(iii) Emitter base junction is reverse bias collector base junction is forward bias

(iv) Emitter base junction is forward bias collector base junction is reverse bias.

Ans. (iv) Emitter base junction is forward bias collector base junction is reverse bias.

Q.1. (d) An amplifier circuit of voltage gain 100, 2V output voltage the input voltage applied is ....

Ans. 0.02 V

Q.1. (e) In enhancement n-channel MOSFET an induces n type channel can be produced between the source and drain if V_{gs} is negative.

Ans. False

Q.1. (f) Inverting amplifier gain is independent of source resistance.

Ans. True

Q.1. (g) The output voltage in OPAMP differentiator with input voltage V_i the output voltage is given by .... when $R = 1\ K$ and $C = 1$ pf.

Ans. $-10^{-9}\dfrac{dv_i}{dt}$

Q.1. (h) $(CA95.12)_{16} - (9FE.A)_{16} = ...$

Ans. C096.72

Q.1. (i) $A'B'C' + A'B'C + A'BC' + ABC' = $ ....

Ans. $A'B' + BC'$

Q.1. (j) The sweep voltage is applied on the .... axis of CRO.

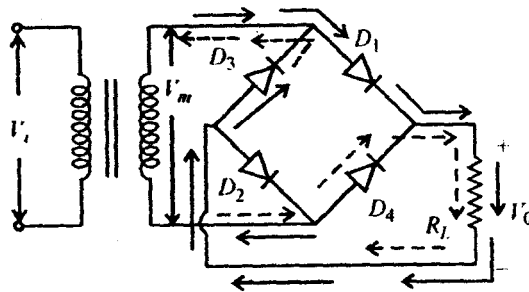Ans. horizontal

Q.2. Attempt any for parts: (5×4=20)

(a) Draw the circuit diagram of full wave bridge rectifier and explain the operation and also draw the input and output waveform.

Ans. During + ve cycle of input:

D_1 & D_2 are ON

D_3 & D_4 are OFF

The direction of current through R_L is as shown by ($\rightarrow$) line.

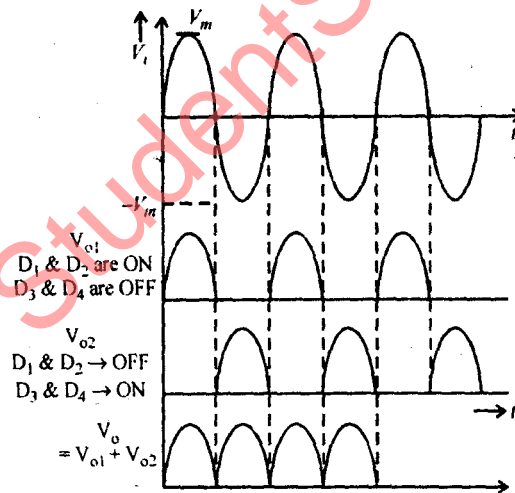**During – ve cycle of input:**

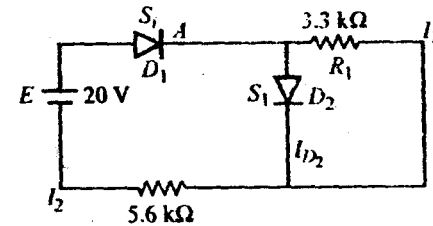D_1 & D_2 are OFF

D_3 & D_4 are ON

The direction of current through R_L is as shown ($\cdots\rightarrow$) by line.
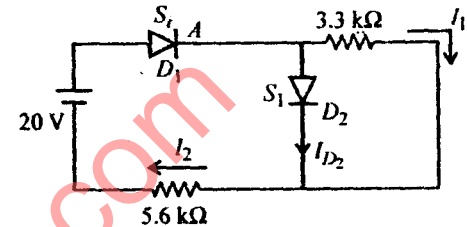
The direction of current is same in both cycle.

The waveforms are as shown in the diagrams.

(b) Determine the current I_1, I_2 and ID_2 for the network shown below (Fig.)

Ans.

D_1 and D_2 both will be ON. Since it is Si diode drop will be 0.7 V

$\therefore \qquad I_1 = \dfrac{V_{D_2}}{3.3\,K} = \dfrac{0.7}{3.3\,K} = 0.212\ mA$

Applying KVL in Ist loop

$E - V_{D_1} - V_{D_2} - V_{5.6\,K} = 0$

$\therefore$ Drop across 5.6 K i.e.
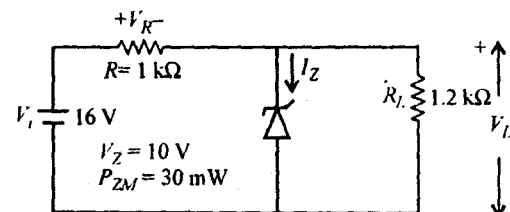
$V_{5.6\,K} = 20 - 0.7 - 0.7\ V = 18.6\ V$

Now $V_{5.6\,K} = I_2 \times 5.6\ K$

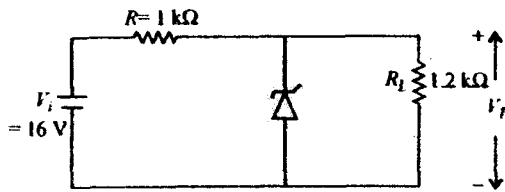$\Rightarrow \qquad I_2 = \dfrac{18.6}{5.6\,K} = 3.32\ mA$

Now $\qquad I_2 = I_{D_2} + I_1$

$\Rightarrow \qquad I_{D_2} = 3.32 - 0.212 = 3.108\ mA.$

(c) For the Zener diode network of the fig. determine V_L, V_R, I_Z and P_Z.

Ans. Step 1: Removing Zener diode from the circuit and solving for V_L.
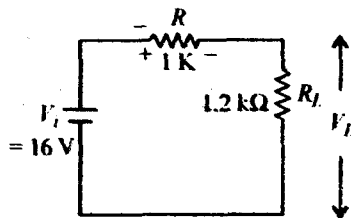
Case (i): If $V_L > V_Z$ then Zener diode is ON

Case (ii): If $V_L > V_Z$ then Zener diode is OFF

$$\therefore \quad V_L = \frac{V_i \times R_L}{R \times R_L} = \frac{16 \times 1.2}{1 + 1.2} = 8.72 \text{ V}$$

Since $V_L < V_Z$ hence Zener diode is off, now the circuit is
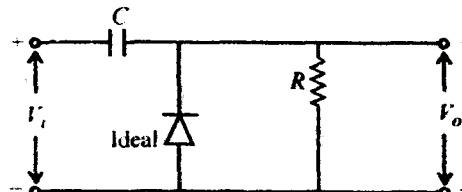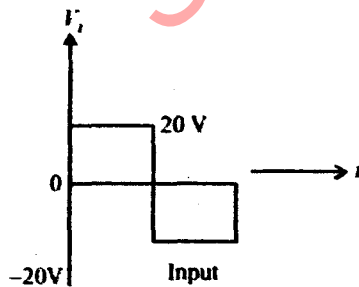

From the figure:

$$I_Z = 0$$
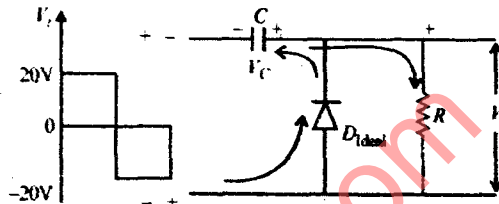$$V_L = 8.72 \text{ V}$$
$$P_Z = 0$$

$$I = I_R = \frac{16}{1 + 1.2 \, K} = 7.27 \text{ mA}$$

$$\therefore \quad V_R = I_R \times 1K$$
$$= 7.27 \times 10^{-3} \times 1 \times 10^3$$
$$= 7.27 \text{ V}$$

(d) Sketch V_o for the network of fig. 3 for the input shown:

Ans. The diode is on during (– ve) cycle

During – ve cycle of input: Diode → ON, Capacitor starts charging with polarity as shown.
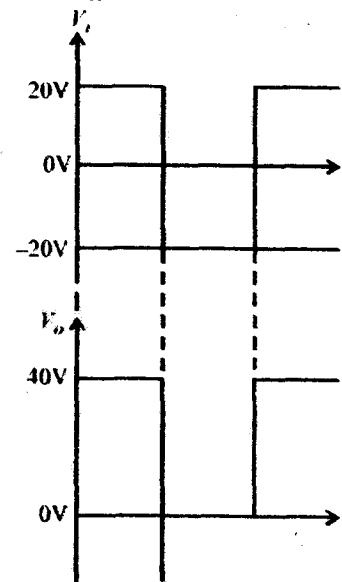
$$V_C = + 20 \text{ V}, \quad V_o = 0$$

During + ve cycle: Diode → OFF Capacitor starts working as battery and discharge through 'R'.
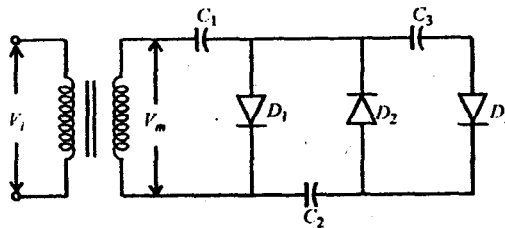
Applying KVL:

$$V_C - V_R + V_i = 0$$
$$+ 20 \, V - V_R + 20 = 0$$
$$V_R = 40 \text{ V}$$

(e) **Draw the voltage Tripler circuit and explain the operation.**

Ans. Voltage Tripler Circuit:

During + ve cycle of input:

$D_1 \rightarrow$ forward biased D_2 & $D_3 \rightarrow$ OFF

$C_1 \rightarrow$ Charges to V_m

$\therefore V_{C_1} = + V_m$

During – ve cycle of input:

D_2 & D_3 are OFF $D_2 \rightarrow$ ON

$C_1 \rightarrow$ holds the voltage V_{in}

Applying KVL

$-V_{C_2} + V_{C_1} + V_i = 0$

$-V_{C_2} + V_m + V_m = 0 \Rightarrow V_{C_2} = 2V_m$

During next + ve cycle

D_1 & $D_2 \rightarrow$ reverse biased, hence OFF $D_3 \rightarrow$ ON

$V_{C_1} = V_m, \; V_{C_2} = 2V_m$

Applying KVL to the outer loop:

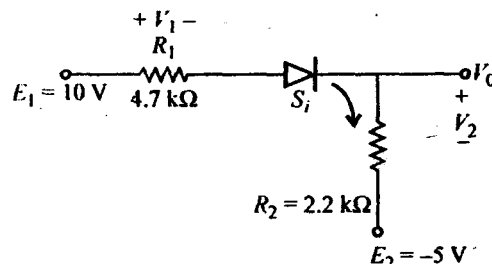$+V_i - V_{C_1} - V_{C_3} + V_{C_2} = 0$

$V_{C_3} = V_i - V_{C_1} + V_{C_2} = V_m - V_m + 2V_m$
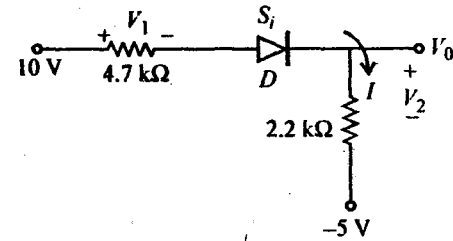
$\Rightarrow V_{C_3} = 2V_m$

V_o is taken across cap. C_1 & C_3

Hence $V_o = V_{C_1} + V_{C_3} = V_m + 2V_m = 3V_m$

(f) **Determine I, V_1, V_2 and V_0 for the series of dc configuration in fig.**

Ans. $10V - I \times 4.7\,K - V_D - I \times 2.2K + 5V = 0$

$I = \dfrac{10 + 5 - 0.7V}{4.7K + 2.2K} = 2.07\ mA$

$V_1 = I \times 4.7\,K$

$\quad = 2.07 \times 4.7 = 9.73\ V$

$V_2 = I \times 2.2\,K$

$\quad = 2.07 \times 2.2 = 4.55\ V$
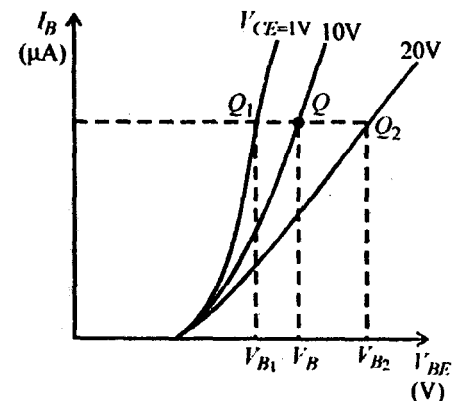
$V_o - V_2 + E_2 = 0$

$V_o = V_2 - E_2$

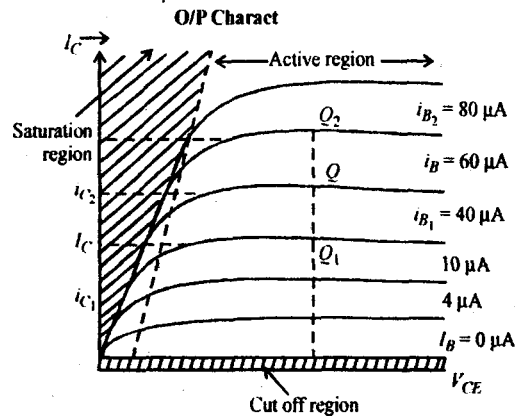$\quad = 4.55 - 5V = -0.45\ V$

Q.3. Attempt any two parts: (10×2=20)

(a) **Draw the input and output characteristics ($v - i$) of a CE npn transistor configuration with proper levels and discuss how you will determine h_{ie} and h_{fe} hybrid parameters from these characteristics.**

Ans. I/P and Output characteristics of npn transistor (CE):

I/P charact:

O/P Charact

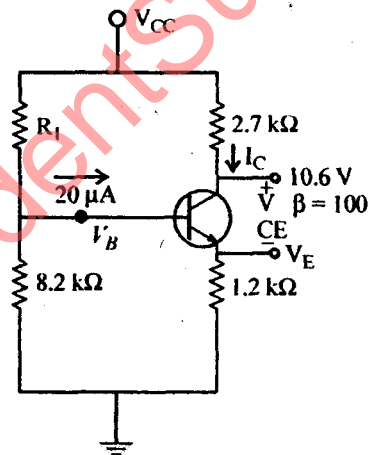**Determination of h_{ie} and h_{fe} from above charact:**

$$h_{fe} = \frac{\delta i_C}{\delta i_B} = \frac{\Delta i_C}{\Delta i_B}\bigg|_{V_C} = \frac{i_{C_2} - i_{C_1}}{i_{B_2} - i_{B_1}} \quad \text{(from output charact)}$$

$$h_{ie} = \frac{\delta V_B}{\delta i_B} = \frac{\Delta V_B}{\Delta i_B}\bigg|_{V_C} \quad \text{(from i/p charact)}$$

(b) For the voltage-divider bias confiration of fig. determine (i) I_C (ii) V_E (iii) V_{CC} (iv) V_{CE} (v) V_B (vi) R_1

Ans. $I_B = 20\ \mu A$

(i) $I_C = \beta I_B = 100 \times 20 \times 10^{-6} = 2\ mA$

$I_E \approx I_C = 2\ mA$

(ii) $V_E = 2 \times 1.2 = 2.4\ V$

(iii) $V_{CE} = V_C - V_E = 10.6 - 2.4\ V = 8.2\ V$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

(iv) $V_{CC} = V_{CE} + I_C(R_C + R_E) = 8.2 + 2(2.7 + 1.2) = 16\ V$

(v) $V_{BE} = V_B - V_E$

$\Rightarrow$ $V_B = V_{BE} + V_E = 0.7 + 2.4$ V $= 3.1$ V
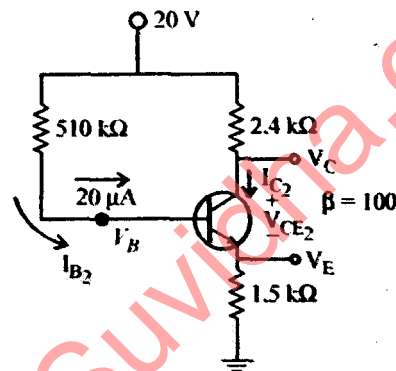
(vi) $V_B = \dfrac{R_2 V_{CC}}{R_1 + R_2}$
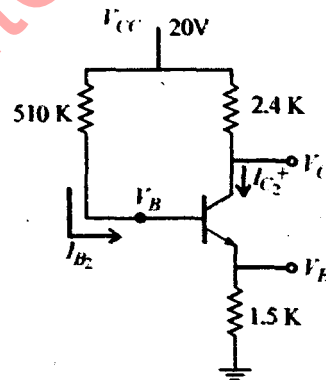
$\Rightarrow$ $3.1(R_1 + R_2) = R_2 \times 16$ V

$R_1 + 8.2\text{K} = \dfrac{8.2 \times 16}{3.1}$

$R_1 = 34.12 \text{ k}\Omega$

(c) For the emitter-stabilized bias circuit of fig., determine (i) I_{B_2} (ii) I_{C_2} (iii) V_{E_2} (iv) V_C (v) V_B (vi) V_E

Ans. Applying KVL in Base:

$V_{CC} - I_{B_2} R_B - V_{BE} - I_E R_E = 0$

Putting $I_E = (1 + \beta) I_{B_2}$

$\therefore$ (i) $I_{B_2} = \dfrac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} = \dfrac{20 - 0.7 V}{510 + (101)2.4} = \dfrac{19.3}{752.4} = 0.02565$ mA

(ii) $I_{C_2} = \beta I_{B_2} = 100 \times 0.02565 = 2.565$ mA

Applying KVL to C-E loop:

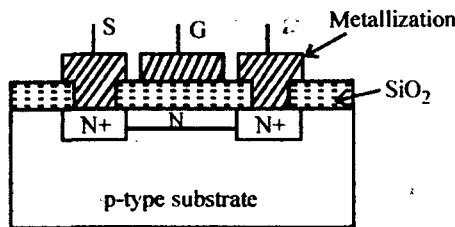$$V_{CC} - I_{C_2}R_C - V_{CE_2} - I_E R_E = 0 \quad I_E \approx I_{C_2}$$

$(iii) \therefore \quad V_{CE_2} = V_{CC} - I_{C_2}(R_C + R_E)$

$$= 20 - 2.565(2.4 + 1.5) = 9.9965 \text{ V}$$

$(iv) \quad V_{CE_2} = V_C - V_E$

$\Rightarrow \quad V_C = V_{CE_2} + V_E = 9.9965 + 3.8475 = 13.844 \text{ V}$

$(v) \quad V_{BE} = V_B - V_E$

$\Rightarrow \quad V_B = V_{BE} + V_E = 0.7 + 3.8475 \text{ V} = 4.5475 \text{ V}$

$(vi) \quad V_E = I_E R_E = I_{C_2} \times R_E = 2.565 \times 1.5 = 3.8475 \text{ V}$
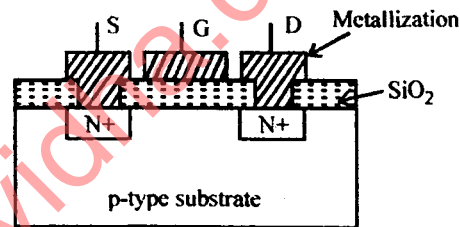
Q.4. Attempt any two parts: (10×2=20)

(a) What is the significant difference between the construction of an enhancement-type MOSFET and depletion-type MOSFET? Sketch the basic construction of a *p*-channel depletion-type MOSFEt.
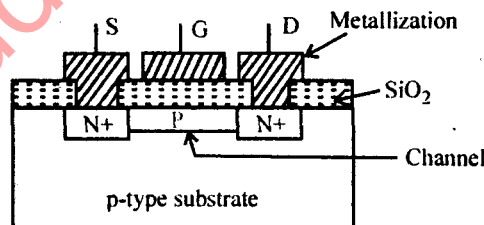
Ans.

Depletion type   **Enhancement type**

The main difference between the construction of depletion type and enhancement type MOSFEt is that in E-MOSFET substrate extends all the way to the SiO_2 and no channels are doped between the source and drain whereas in De-MOSFET channel is formed by diffusion between source and drain.

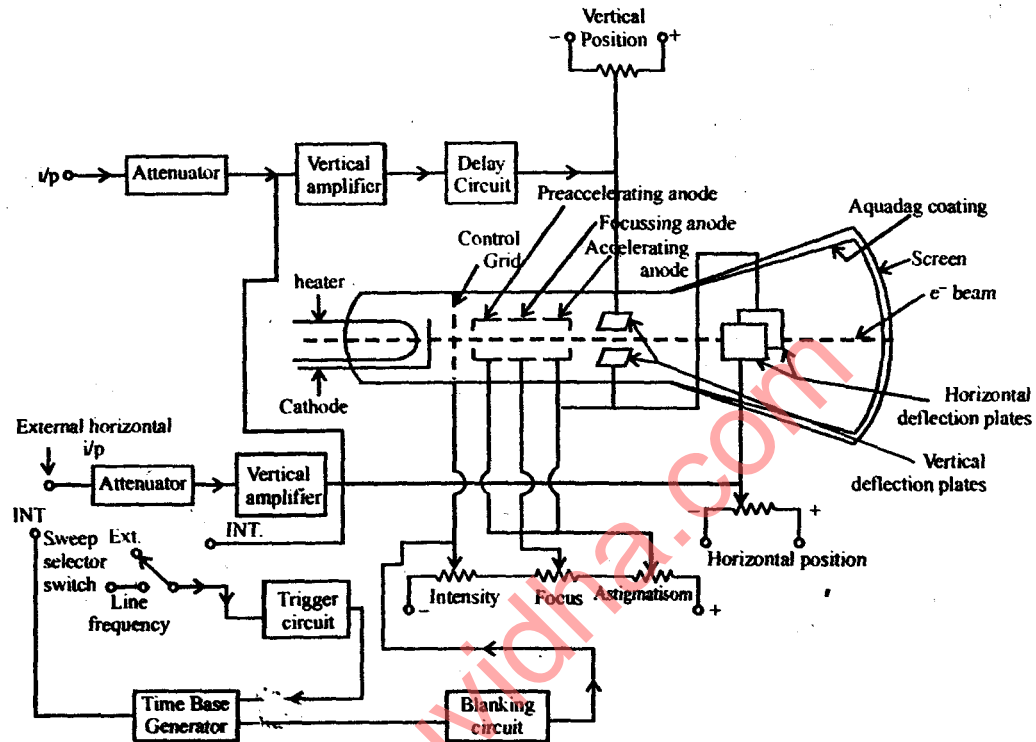**P-Channel Depletion Type MOSFET:**

$S \rightarrow$ Source
$G \rightarrow$ Gate
$D \rightarrow$ Drain

(b) Draw a neat schematic diagram of a cathode ray tube with proper labels. How is the intensity of the spot/trace controlled in a cathode ray oscilloscope?
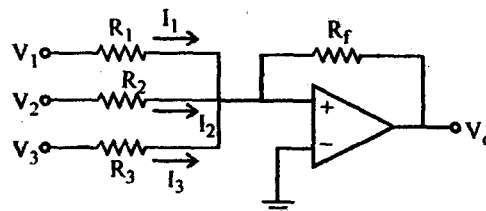
Ans.

The potential of the control grid w.r.t cathode is controlled with the help of potentiometer in order to control the intensity or brightness of spot.

   (c) (i) Sketch a three-input inverting summing circuit and derive an expression for the output voltage.

   (ii) Design a non-inverting amplifier circuit that is capable of providing a voltage gain of 15. Assume ideal op-amp and resistances used should not exceed 30 kΩ.
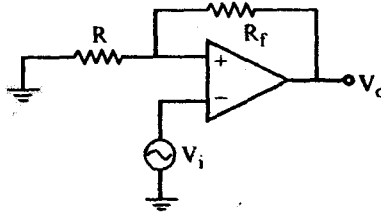
Ans. (i) Applying KCL,

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = \frac{V_A - V_o}{R_f}$$

Since V_A = Vertical ground = 0

$$\therefore \quad \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_f}$$

$\therefore$

and if $R_1 = R_2 = R_3 = R_f$ then $V_o = -[V_1 + V_2 + V_3]$

(ii) Gain of noninverting amplifier, $A_V = 1 + \dfrac{R_f}{R}$

Given $\quad A_V = 15$

$$\therefore \quad 15 = 1 + \frac{R_f}{R}$$

$$\therefore \quad \boxed{R_f = 14R}$$

Let $\quad R = 1.2\ k\Omega,$

then $\quad R_f = 14 \times 1.2 = 16.8\ k\Omega$

Q.5. Attempt any four parts: (5×4=20)

(a) Simplify the following functon by using Boolean algebra:

(i) $A\bar{B}\bar{C}D + \bar{A}\bar{B}D + BC\bar{D} + \bar{A}B + B\bar{C}$

(ii) $(AB + \bar{A}C + BC)(A + \bar{B} + A\bar{B})$

Ans. (i) $A\bar{B}\bar{C}D + \bar{A}\bar{B}D + BC\bar{D} + \bar{A}B + B\bar{C} = \bar{B}D[\bar{A} + A\bar{C}] + B[\bar{C} + C\bar{D}] + \bar{A}B$

$$= \bar{B}D[\bar{A} + \bar{C}] + B[\bar{C} + \bar{D}] + \bar{A}B$$

$$= \bar{A}\bar{B}D + \bar{B}\bar{C}D + B\bar{C} + B\bar{D} + \bar{A}B$$

$$= \bar{A}[B + \bar{B}D] + \bar{C}[B + \bar{B}D] + B\bar{D}$$

$$= \bar{A}[B + D] + \bar{C}[B + D] + B\bar{D}$$

$$= \bar{A}B + \bar{A}D + B\bar{C} + \bar{C}D + B\bar{D}$$

(ii) $(AB + \bar{A}C + BC)(A + \bar{B} + A\bar{B}) = AB + AB\bar{B} + AB\bar{B} + A\bar{A}C + ABC + A\bar{A}\bar{B}C$

$$+ ABC + B\bar{B}\bar{C} + A\bar{B}BC$$

$$= AB + \bar{A}\bar{B}C + ABC$$

$$= AB[1 + C] + \bar{A}\bar{B}C = AB + \bar{A}\bar{B}C$$

(b) Perform the following binary arithmetic operations:

(i) $(1101.1101)_2 - (1001.10)_2$

(ii) $(AB9.54)_{16} + (39C.CD)_{16}$

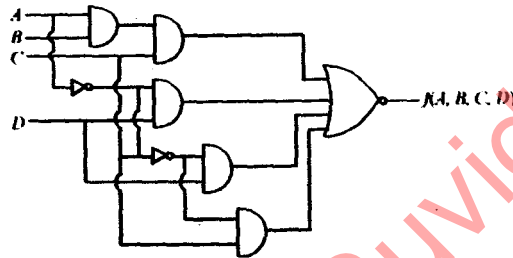**Ans.** $(i)\,(1101.1101)_2 - (1001.10)_2 = (0100.0101)_2$

$(ii)\,(AB9.54)_{16} + (39C.CD)_{16} = (2117.11)_{16}$

(c) Simplify the function using K-map:

$f(A, B, C, D) = \Sigma m(3, 4, 5, 7, 9, 13, 14, 15) + \Sigma d(0, 1, 8, 10)$

Implement the output using gates.

Ans. $f(A, B, C, D) = \Sigma m(3, 4, 5, 7, 9, 13, 14, 15) + \Sigma d(0, 1, 8, 10) = ABC + \bar{A}D + \bar{C}D + \bar{A}\bar{C}$

(d) (i) Convert the given expression into canonical SOP form:

$f = A + AB + ABC$

(ii) Convert the given expression into canonical POS form:

$f = (A + B)(B + C) + (C + A)$

Ans. $f = A + AB + ABC$

$$= A(B + \bar{B})(C + \bar{C}) + AB(C + \bar{C}) + ABC$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + ABC + AB\bar{C} + ABC$$

$$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C}$$

(ii)

$$f = (A + B)(B + C) + (C + A)$$

$$= AB + AC + B + BC + A + C$$

$$= B[A + 1] + A[C + 1] + C[B + 1]$$

$$= (A + B + C).$$

or Question is

$$f = (A + B)(B + C) + (C + A)$$

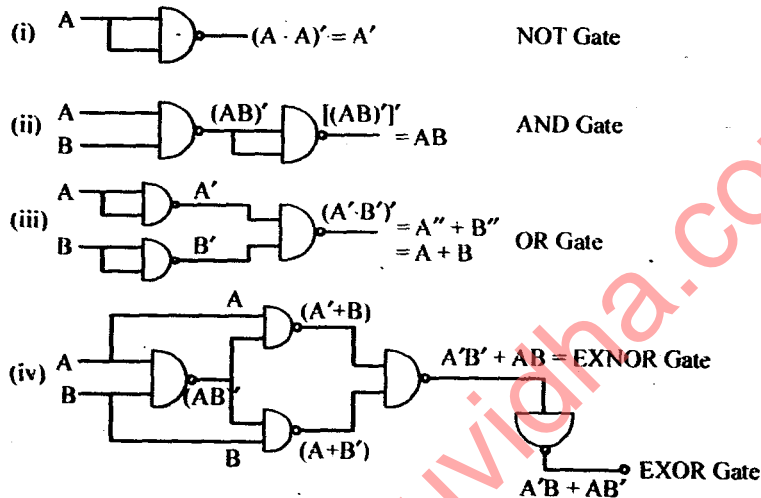$$= (A + B + C\bar{C})(A\bar{A} + B + C)(A + B\bar{B} + C)$$

$$= (A + B + C)(A + B + \bar{C})(A + B + C)\ (\bar{A} + B + C)(A + B + C)(A + \bar{B} + C)$$

$$= (A + B + C)(A + B + \bar{C})(\bar{A} + B + C)\ (A + \bar{B} + C)$$

(e) What is the universal gate? Name the universal gate? Give the proof of universal gate at least for one type of gate.
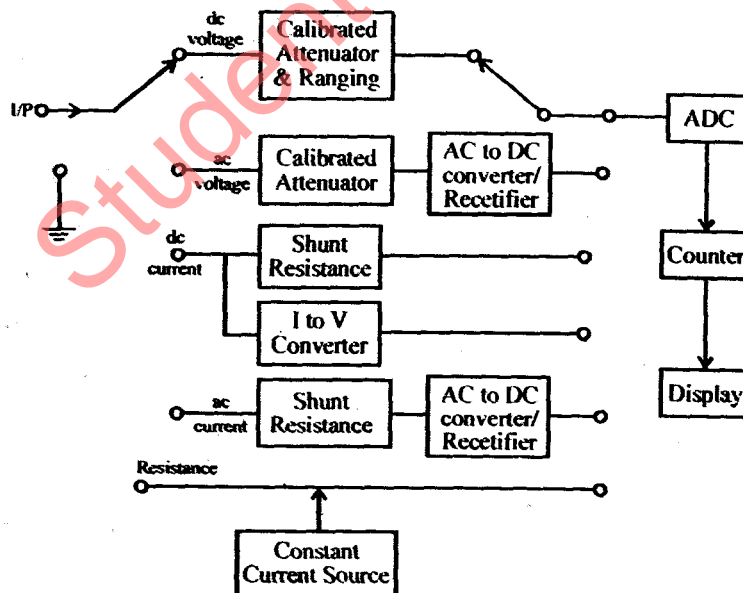
Ans. Universal Gate: These are those gates from which all other basic and special purpose gate boolean expressions can be obtained. NAND and NOR gates.

NAND Gate:

(i) A — $(A \cdot A)' = A'$ — NOT Gate

(ii) A, B — $(AB)'$ — $[(AB)']' = AB$ — AND Gate

(iii) A → A', B → B' — $(A' \cdot B')' = A'' + B'' = A + B$ — OR Gate

(iv) A, B — $(A'+B)$, $(AB)'$, $(A+B')$ — $A'B' + AB$ = EXNOR Gate — $A'B + AB'$ = EXOR Gate

(f) Draw the block diagram of digital multimeter. explain the operation of each block.

Ans. Digital Multimeter:

DC voltage and current are passed through attenuator for proper ranging of instrument and then converted into digital form by ADC and then to display.

AC voltage and current are passed through ac to dc converter to convert then into voltage and then again to ADC and to display. Current is passed through shunt resistance. Voltage drop across it is measured.

Thirdly a constant current is pased through unknown resistance, voltage drop across it is measured through display.