# B.TECH.    EEC-101/201

## SECOND SEMESTER THEORY EXAMINATION, 2009-10

## ELECTRONICS ENGINEERING

*Time : 2 Hours*                                    *Total Marks : 100*

*Attempt All questions.*

### SECTION-A

Attempt all parts of this question. All parts of the question carry equal marks.

This question contains 10 objective type/fill in the blank type/true-false type questions. Select most appropriate option.

(a) When we apply reverse bias to a junction diode, it :

   (i) lowers the potential barrier.

   (ii) raises the potential barrier.

   (iii) greatly decreases the minority-carrier current.

   (iv) greatly increases the majority-carrier current.

Ans. (ii) raises the potential barrier.

(b) Ripple frequency of the output wave form of the a full-wave rectifier when fed with a 50 Hz sine wave is :

   (i) 25 Hz

   (ii) 50 Hz

   (iii) 100 Hz

   (iv) 200 Hz

Ans. (iii) 100 Hz

(c) "An ordinary transistor is called 'Bipolar Junction Transistor' because it has two poles-one positive and the other negative". The statement is :

   (i) True

   (ii) False

Ans. (ii) False.

(d) The transistor configuration which provides highest output impedance is :

   (i) Common Base

   (ii) Common Emitter

   (iii) Common Collector

   (iv) None of the above

Ans. (i) Common Base

(e) In a Field Effect Transistor (FET) the gate to source voltage that gives zero drain current is called ......... voltage.
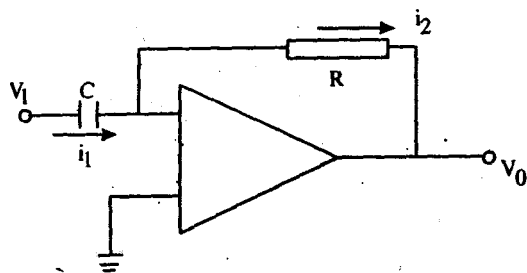
Ans. Cut-off

(f) When the positive voltage on the gate of a p-channel JFET is increased, its drain current :

   (i) increases

   (ii) decreases

   (iii) remains the same

   (iv) none of the above

Ans. (ii) decreases

(g) For the circuit shown in Figure-1., the output voltage $v_0$ is given by :

(i) $v_0 = -\dfrac{1}{RC}\dfrac{dv_i(t)}{dt}$

(ii) $v_0 = -\dfrac{1}{RC}\displaystyle\int_0^t v_i(t)\,dt$

(iii) $v_0 = -RC\dfrac{dv_i(t)}{dt}$

(iv) $v_0 = -RC\displaystyle\int_0^t v_i(t)\,dt$

**Ans.** $v_0 = -RC\dfrac{dv_i(t)}{dt}$

**(h)** Three Boolean operators are :

(i) NOT, OR, AND

(ii) NOT, NAND, OR

(iii) NOR, OR, NOT

(iv) NOR, NAND, NOT

**Ans.** (i) NOT, OR, AND

**(i)** Lissajous pattern obtained on the screen of a CRO can be used to determine :

(i) Phase shift

(ii) Amplitude distortion

(iii) Voltage amplitude

(iv) None of the above

**Ans.** (i) Phase shift

**(j)** "A digital voltmeter has negligible loading effect on the circuit under test because its input resistance is very high". The above statement is :

(i) True

(ii) False

**Ans.** (i) True

## SECTION-B

2. Attempt any three parts of the following :

**(a) (i)** Describe the conditions established by forward and reverse-bias conditions on a p-n junction diode and how the resulting current is affected.

**Ans.** When the diode is forward-biased and the applied voltage is increased from zero, hardly any current flows things the device in the beginning. It is so because the external voltage is being opposed by the internal barrier voltage $V_B$ whose value is 0.7 V for Si and 0.3 V for Ge. As soon as $V_B$ is neutralised, current through the diode increase rapidly with increasingly applied battery voltage.

When the diode is reverse-biased, majority carriers are blocked and only a small current (due to minority carriers) flows through the diode. As the reverse voltage is increased from zero, the reverse current very quickly reaches its maximum or saturation value $I_0$ which is also known as leakage current.
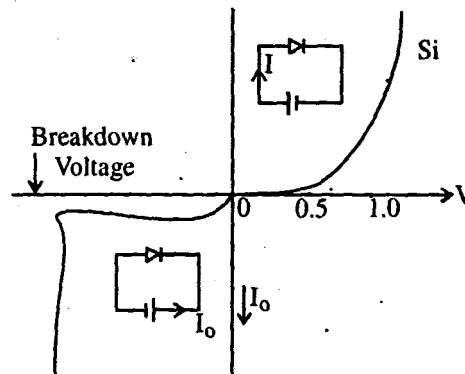
The diode is said to be in reverse bias when the potential barrier increases during reverse biasing.

The current doesn't flow in the circuit because the electrons repel the flow and theoretically no current flows but practically a small current flows due to minority charges.

**(ii)** **Calculate forward current $I_F$ for the silicon diode with dynamic resistance $r_d = 0.25\Omega$ used in the following circuit of Figure-2.**



**Ans.**
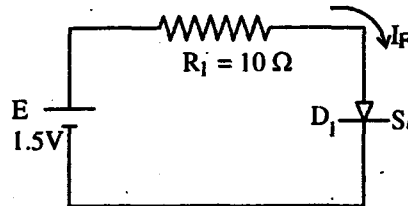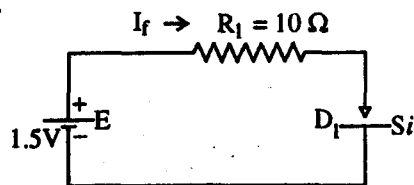


$$I_f = \frac{(1.5-0.7)}{(10+.25)} \Rightarrow I_f = \frac{0.8}{10.25}$$

$$I_f = 0.07804\,A \Rightarrow \boxed{I_f = 78.04\,mA}$$

**(b)** **(i)** **What is major difference between a bipolar and an unipolar device? Explain with example.**

**Ans.**

| Bipolar device | Unipolar device |
|---|---|
| 1. Current in the device is carried by both electrons and holes | 1. Current in the device is carried either by electrons or holes. |
| 2. It is a current controlled device i.e. the base current controls the amount of collector current. | 2. It is a voltage controlled device i.e., voltage at the gate terminal controls the amount of current. |
| 3. Its input resistance is very low | 3. Its input resistance is very high |
| 4. It has positive temperature coefficient of temperature. | 4. It has negative temperature coefficient at high current level. |
| 5. It is comparatively more noisy than unipolar device | 5. It is less noisy |
| 6. It is comparatively difficult to fabricate e.g., BJT (Bipolar Junction Transistor) | 6. It is much quite easy to fabricate e.g. FET (Field effect transistor) |

**(ii) Draw and explain the input and output characteristics of common base configuration using npn bipolar junction transistor. Indicate all the region of operations.**

**Ans. Input characteristics :**
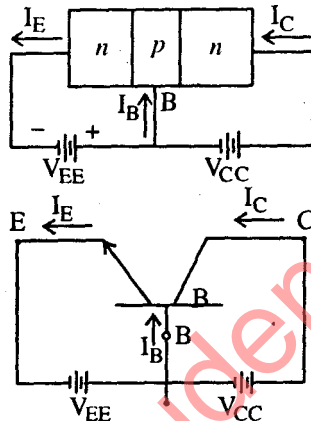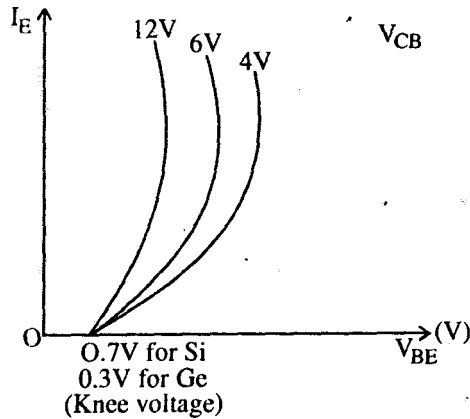


1. It is plotted between input current and input voltage with output voltage constant.
2. Below the cut in voltage the emitter current is negligibly small. ∴ Knee voltage is there.
3. A fter the Knee voltage, the emitter current, $I_E$ increases rapidly with a small increase in voltage.
4. Input resistance :

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}\Big|_{V_{CB}\ constant}$$

5. With increase in $V_{(B)}$ current shift upwards. Hence input resistance decreases.

**Output characteristics :**
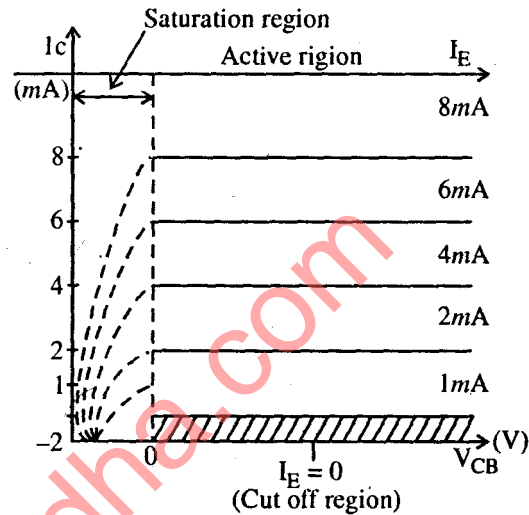


1. It is plotted between output voltage and output current taking input current constant.
2. There are three regions:
   (*i*) Active region
   (*ii*) Saturation region
   (*iii*) Cut off region.
3. In active region, $I_E$ is nearly equal to $I_C$, this shows that it has high output resistance.
4. When the junctions are forward bias, the $I_C$ increases largely with a small increase in voltage ($V_{BC}$).
5. In cut off region, $I_E = 0$ but $I_C$ is not equal to zero because there is a small leakage current.
6. Output resistance:

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}\Big|_{I_E\ constant}$$
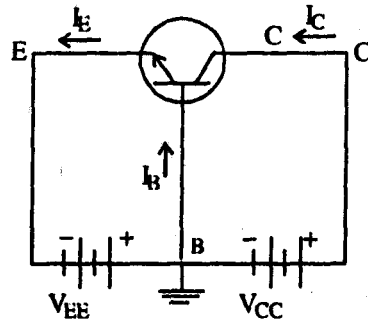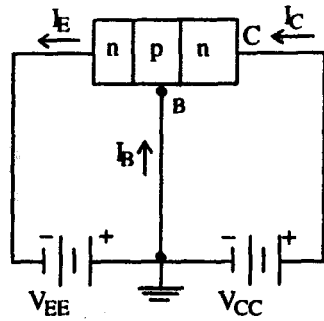
→ Notation & symbols with the common base configuration ($n \phi n$)

**(c) (i) What are the advantages of FET over BJT? Explain.**

**Ans. Advantages of FET over BJT :** High input impedance, small size, high frequency response, low noise, negative temperature coefficient, hence better thermal stability, high power gain, No off. voltage when used as switch.

**(ii) Derive expression for voltage gain of inverting and non-inverting ideal operational amplifier configurations.**

**Ans. For inverting amplifier :**
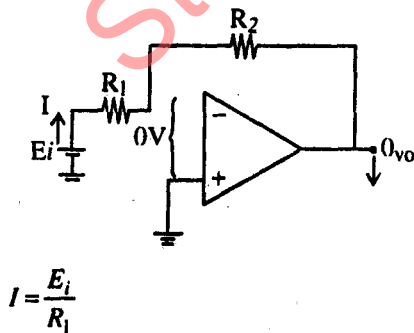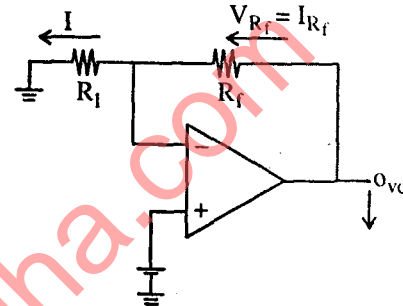


$$I = \frac{E_i}{R_1}$$

$$V_{Rf} = I \times R_f = \frac{E_i}{R_i} R_f.$$

$$V_{out} = V_{Rf}. \left(\text{Voltage across } R_f\right)$$

$$V_{out} = - E_i \frac{R_f}{R_i}$$

**Open loop gain** $= A_{CL} \quad \dfrac{V_0}{E_i} = -\dfrac{R_F}{R_1}$

**For Non-inverting amplifier**



$$I = \frac{E_i}{R_1}$$

$$V_{R_f} = I\left(R_f\right) = \frac{R_f}{R_1} E_i$$

$$V_o = E_i + \frac{R_f}{R_1} E_i$$

[The output voltage $v_o$ is found by adding the voltage drop across $R_1$, which is $E_i$, and voltage $V_{R_f}$ ]

$$V_o = \left(1 + \frac{R_f}{R_1}\right) E_i$$

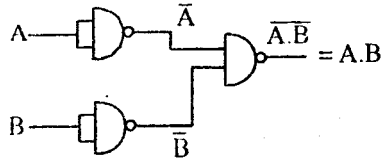or $\boxed{\dfrac{V_o}{E_i} = 1 + \dfrac{R_f}{R_1}}$

**(d) (i) What are universal gates? Why they are called so? Justify your answer.**

**Ans.** NAND and NOR gates are universal. OR gates, we can construct all the gates with the help of these gates, so it is called universal gates.
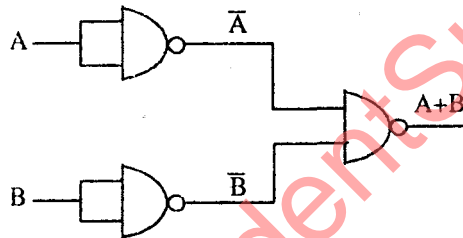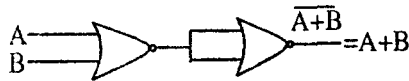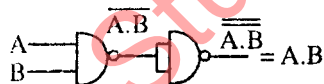
**NAND as NOT**

A—[NAND]— $\bar{A}$

**NAND as OR gate**

A—[NAND]— $\bar{A}$
B—[NAND]— $\bar{B}$
→[NAND]— $\overline{\bar{A}.\bar{B}}$ = A.B

**NOR as NOT**

A—[NOR]— $\bar{A}$

**NOR as OR gate**

A, B —[NOR]—[NOR]— $\overline{\overline{A+B}}$ = A+B

A—[NAND]— $\bar{A}$
B—[NAND]— $\bar{B}$
→[NOR]— A+B

**NAND as AND gate**

A, B —[NAND]— $\overline{A.B}$ —[NAND]— $\overline{\overline{A.B}}$ = A.B

**NAND as Ex – OR**

A, B —[NAND gates network]— A⊕B

**NOR as AND gate**

A—[NOR]— $\bar{A}$
B, R—[NOR]— $\bar{B}$
→[NOR]— $\overline{\bar{A}+\bar{B}}$
=A–B

**NOR as EX OR**

A, B —[NOR gates network]— A⊕B
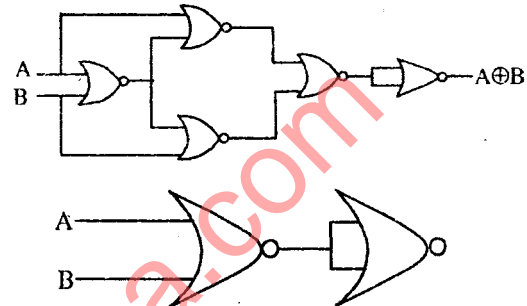
A, B —[OR / gate network]—
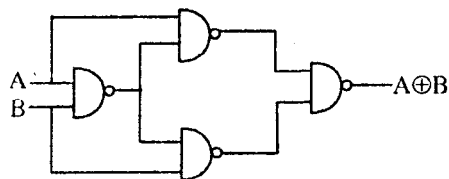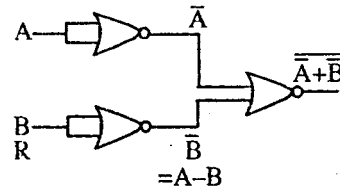
**(ii) What do you understand by don't care conditions? Is it an advantage or disadvantage to include them in a map? Explain with reasons.**

**Ans. Don't care condition :** Some min. terms or max. terms have not specified value. They are considered as don't care condition and can be represented as 'X' in the K-map.

It is an advantage to include don't care conditions in a MAP because we can form maximum size group using don't care condition which simplify the circuit.

e.g.

| A\BC | | | |
|---|---|---|---|
| 1 | × | 1 | × |
| × | 1 | × | 1 |

Using don't care, we can make a group of 8 in the above example which simplifies the circuit otherwise we get a complicated circuit.

**(e) Draw the block diagram of a CRO and briefly explain the function of each block.**

**Ans. Components of CRO :**

1. **Vertical amplifier :** Vertical amplifier is used to give input signal to the vertical plates. Therefore, it is known as vertical amplifier.

2. **Delay line :** Delay line is connected to delay the time to search to the vertical plates so that signals from both the vertical amplifier and horizontal amplifiers reach at the same time.

3. **Trigger circuit :** Trigger circuit is used to made both the horizontal and input waveforms in the same phase so that they start simultaneously.

4. **Time base generator :** It is used to generate the sawtooth voltage waveform. Its sawtooth voltage waveform generated is passed to the horizontal amplifier.

5. **Horizontal amplifier :** Horizontal amplifier amplifies the low voltage signal or attenuate the high voltage signals.
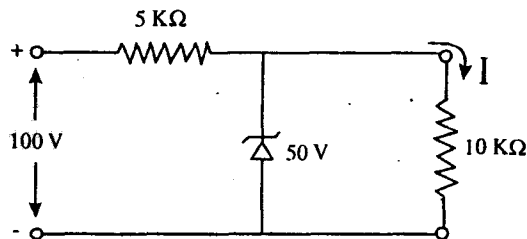


Components of CRO

HV – High Voltage
LV – Low Voltage
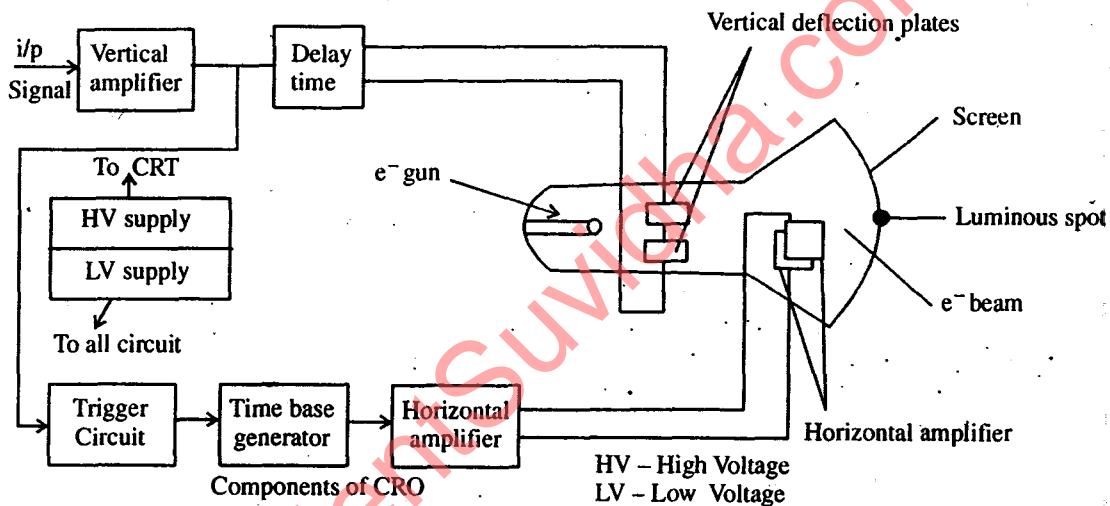
## SECTION-C

**Attempt all questions. All questions carry equal marks.**

3. **Attempt any two part of the following :**

(a) Describe the physical mechanism of Zener breakdown. For the circuit shown in Figure-3, find the voltage drop across the 5Ω resistance.

**Ans. Zener Breakdown :** When a reverse voltage applied to a zener diode it causes a very instance electric field to appear across a narrow depletion region. The electric field intensity of the order of $3 \times 10^5$ V/cm. Such an high electric field is strong enough to pull some of the valence electrons into the conduction band by breaking thin covalent bonds. These electrons then become free electron which are available for conduction. A large number of such free electrons will constitute a large reverse current through the zener diode and breakdown is said to have occurred due to the zener effect.
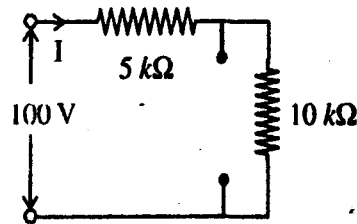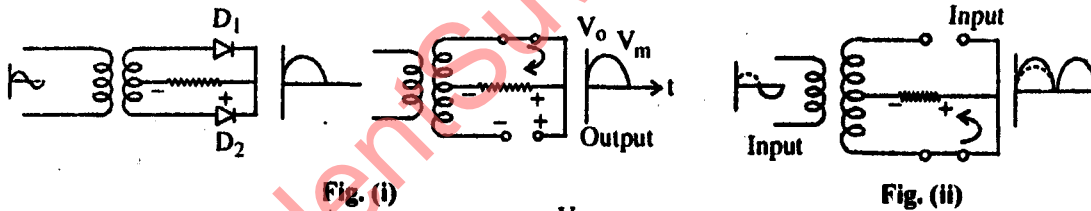


$$I = \frac{100V}{5k + 10k} = 6.67\,mA.$$

and voltage across 10 KΩ resistance $= I \times 10k = 6.67\,mA \times 10 \times 10^3 = 66.7 V$. This voltage is greater than $V_z = 50$. Then the voltage across 10kΩ $= 50\,V$ and across 5kΩ $= 100 - 50 = 50\,V$

**(b)** Sketch a two-diode full wave rectifier circuit for producing a positive output voltage. Sketch the input and output waveforms and explain the circuit operation.

**Ans.**



Fig. (i) Fig. (ii)

During (–ve) cycle $D_1$ is off and $D_2$ is on.
Thus (–ve) cycle will appear across the load.
During + ve cycle $D_1$ is on and $D_2$ is off.
These (+ve) cycle appear across load.
∴ The combined o/p of fig. (i) & fig. (ii) is
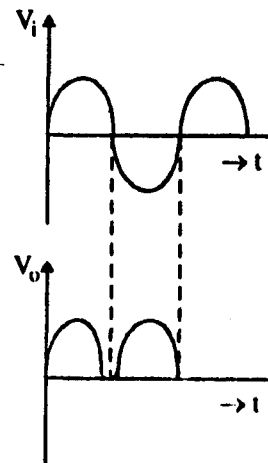
(c) **Draw a voltage doubler circuit. Sketch input and output waveforms and explain the circuit operation.**
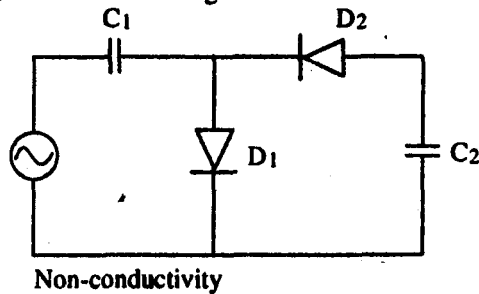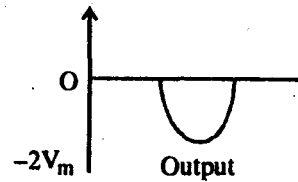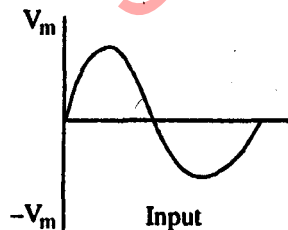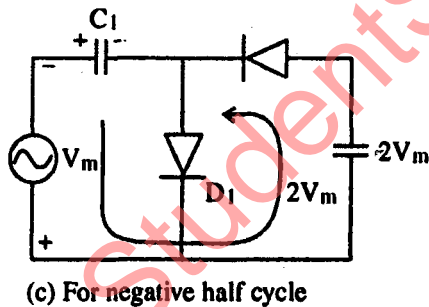
**Ans.** Half wave voltage doubler



Non-conductivity

**Fig. (i) (a)**



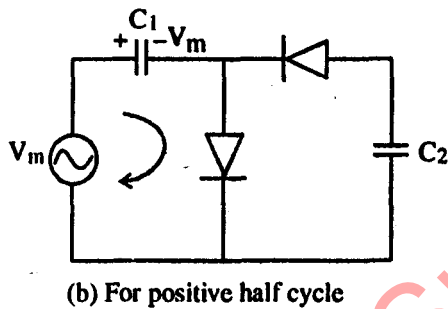(b) For positive half cycle



(c) For negative half cycle
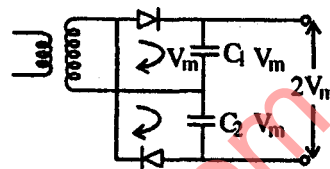


Input



Output

**Full wave voltage Doubler**



**Fig. (ii)**

**For Fig. (i)**

During (+ve) cycle (b)

$D_1 \to$ on $D_2 \to$ off  capacitor ($c_1$) charged to peak voltage of input i.e $V_{c_1} = V_m$

During (−ve) cycle (c)

$D_1 \to$ off $D_2 \to$ on  capacitor $c_2$ starts charging to peak voltage.

Applying KVL to fig. (c)

$$\boxed{V_{c_2} = 2V_m}$$ and $V_o = V_{c_2} = 2V_m$

Fig. (ii)

**During +Ve cycle**

$D_1$ is on and $D_2$ is off

$C_1$ charged to $V_{c_1} = V_m$

**During −Ve cycle**

$D_1$ is off and $D_2$ is on

$C_2$ charged to $V_{c_2} = V_m$

The Vo is taken across $C_1$ and $C_2$ connected in series.

∴ Total $V_o = V_{c_1} + V_{c_2} = 2V_m$

4. Attempt any one of the following :

(a) Derive the expressions for voltage gain, current gain and input impedance in terms of h-parameters for common emitter amplifier.

**Ans.** Current gain $A_i = \dfrac{-i_2}{i_1} = -\dfrac{h_{fe}\, i_1 + h_{oe}\, V_2}{i_1}$

$$= -h_{fe} + h_{oe}\, \dfrac{v_2}{i_1}$$

and $\qquad v_2 = -i_2\, r_L$

$$\therefore \qquad A_i = h_{fe} - h_{oe}\, \dfrac{i_2\, r_L}{i_1}$$

(i)
$$\boxed{A_i = \dfrac{-h_{fe}}{1 + h_{oe}\, r_L}}$$

**Voltage gain**

$$A_v = \dfrac{V_2}{V_1} = \dfrac{V_2}{h_{ie}\, i_1 + h_{re}\, V_2} = -\dfrac{i_2\, r_2}{h_{ie}\, i_1 - h_{re}\, r_2\, i_2}$$

Dividing the numerator and denominator by $i_2$

$$A_v = \dfrac{r_2}{h_{ie}\, \dfrac{i_1}{i_2} - h_{2e}\, r_2} = \dfrac{-r_2}{\dfrac{h_{ie}}{A_i} - h_{fe}\, r_2}$$

Put the value of $A_i$

$$A_v = \dfrac{-r_L}{\dfrac{h_{ie}}{1 + h_{oe}\, r_2} - h_{re}\, r_L} = \dfrac{-h_{fe}\, r_L}{h_{ie} + \left(h_{ie}\, h_{oe} - h_{fe}\, r_L\right)}$$

**Input Impedance**

$$Z_{in} = \dfrac{V_1}{i_1} = \dfrac{h_{ie}\, I_1 + h_{re}\, V_2}{i_1} = h_{ie} + \dfrac{h_{re}\, V_2}{i_1}$$
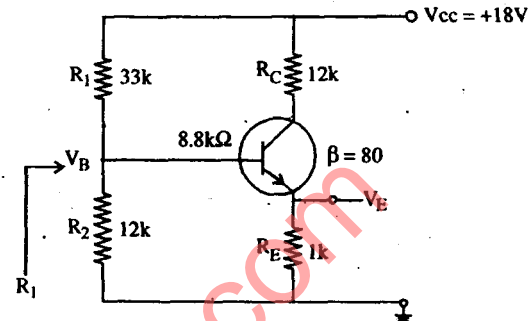
$$V_2 = -i_2 r_2$$

$$Z_{in} = h_{ie} - \dfrac{h_{re}\, r_2\, i_2}{i_1} = h_{ie} - A_i\, h_{re}\, r_2$$

Put the value of $A_i$

$$Z_{in} = h_{ie} - \dfrac{h_{re}\, h_{fe}\, r_2}{1 + h_{oe}\, r_2}$$

(b) Determine the following for the voltage divider bias circuit shown in Figure-5.

(i) $I_C$      (ii) $V_E$

(iii) $V_B$      (iv) $V_{CE}$ and

(v) $R_I$



**Ans.** $R_{TH} = R_1 \parallel R_2 = \dfrac{33\,k\Omega \times 12\,k\Omega}{33k + 12k} = 8.8\,k\Omega$

$$E_{TH} = \dfrac{R_2\, V_{cc}}{R_1 + R_2} = \dfrac{18 \times 12\,k\Omega}{(33 + 12)\,k\Omega} = 4.8\,V$$

If $V_{BE} = 0.7V$

$$I_B = \dfrac{4.8 - 0.7}{(8.8 + 0.7)k} = 0.045\,mA$$

$I_C = 3.65\,mA \qquad V_{CE} = 9.91\,V$
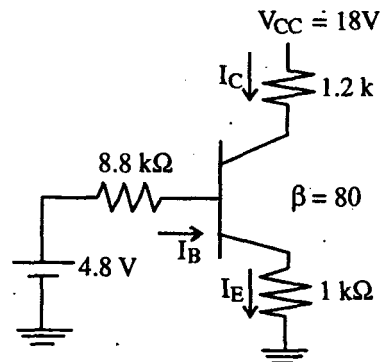
$V_E = 3.69\,V$

$V_B = 4.8\,V.$



**Fig.** $V_{BE} = 0V$

$$I_B = \frac{E_{th} - V_{BE}}{R_{th} + (B+1)R_E} = \frac{4.8 - 0}{8.8k + (81 \times 1k)}$$

$$= \frac{4.8\,V}{89.8\,k\Omega} = 0.053\,mA$$

(i)   $I_C = I_B \times B = 4.27\,mA$

(ii)  $V_E = I_E R_E = (B+1)I_B \times 1k\Omega = 0.053 \times 81 \times 1k\Omega$
$$= 4.29\,V$$

(iii) $V_B = I_1 R_2 = \dfrac{V_{cc}}{R_1 + R_2} - R_2 = 4.8V$

(iv)  $V_{CE} = V_{cc} - I_c(R_c + R_E) + I_B R_E L = 18 - 9.394$
$$= 8.606V - 0.053$$
$$= 8.553\,V$$

(v)   $R_i = R_{th} = 0.8\,k\Omega$

**5.** **Attempt any one of the following :**

**(a)** **Describe the construction and operation of a MOSFET in enhancement mode. Draw its characteristics and equivalent circuit of the device.**
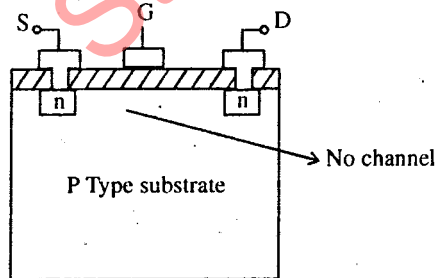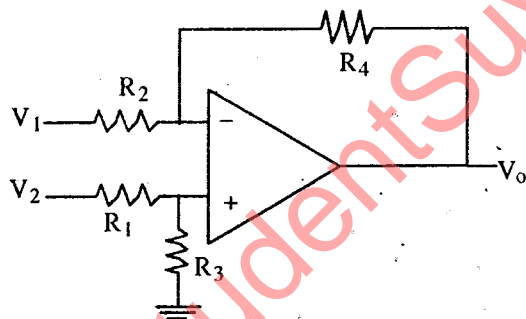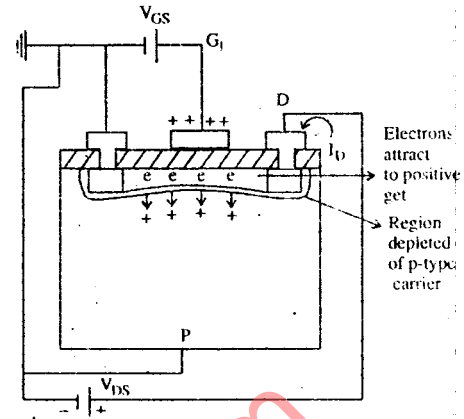


**Ans.**



Fig. (i).



Fig. (ii)

$V_{DS}$. and $V_{GS}$ have been set at some positive voltage greater than $OV'$. The positive potential at the gate will pressure the holes in the p-type substrate along the edge of $S_iO_2$ layer to leave the area and enter deeper region of the p = substrate. The electron's in the p-substrate will be attracted to the positive edge and accumulate in the region near the surface of the $S_iO_2$ layer. The $S_iO_2$ layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As $V_{GS}$ increases in magnitude, the concentration of electronics near the $S_iO_2$ surface incraeases until eventually the induced n-type support a measurable flow between the rain and source.
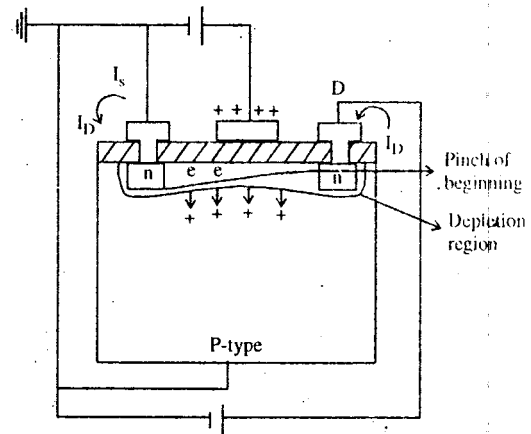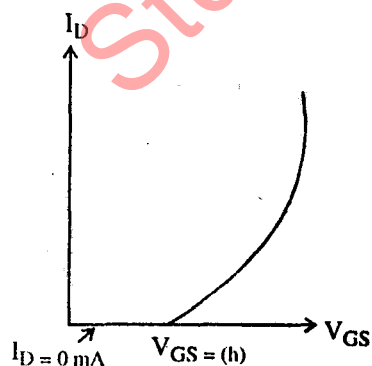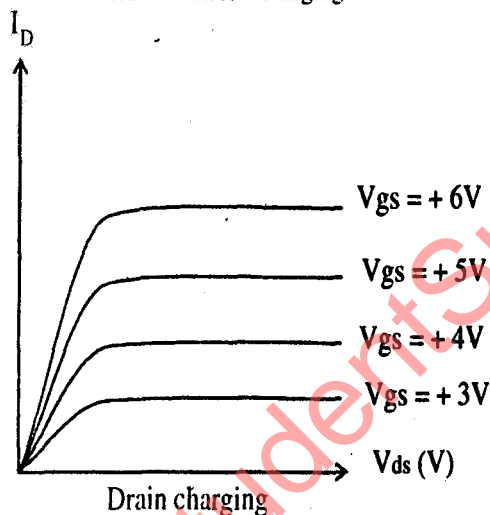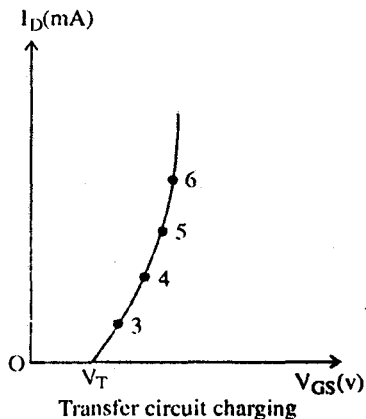


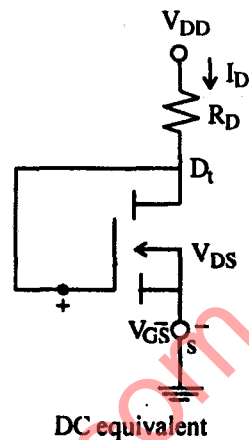Fig. (iii)

If we hold the $V_{c.s}$ constant and increase the level

of $V_{DS}$, the drain current will reach a saturate level. The resulting off of $I_D$ is due to pinch-off process depicted by the narrowing channel and at the drain the inducted channel.



Transfer circuit charging



Drain charging



Transfer characteristic of n channel enhancement type MOSFED



DC equivalent

**(b) (i) Draw the circuit diagram for unity gain amplifier. Where is it used and why?**

**Ans.**
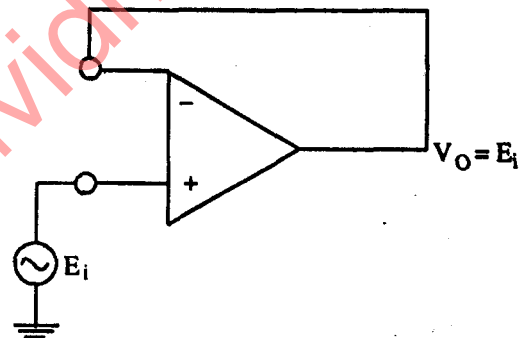


Unity gain amplifier is used because its input resistance is high. Therefore it draws negligible current from a signal source, so the input load effect may be reduced.

A unity gain circuit provides a means of isolating an input from a load and act as ideal circuit with very high input impedance and low output impedance. The advantage of this connection is that the load connected across one output has no effect on the other output.

**(ii) Find the output voltage of the following op-amp circuit shown in Figure.**

**Ans.**
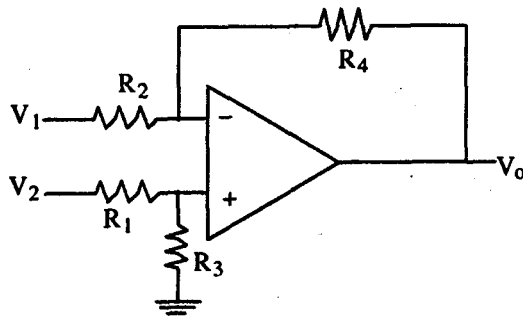


$$V_o = \frac{R_3}{R_1 + R_3} \frac{R_2 + R_4}{R/2} V_2 - \frac{R_4}{R_2} V_1$$

$$V_o = \left[\frac{1}{5+1} \frac{5+10}{5}\right] V_2 - \frac{10\,k\Omega}{5\,k\Omega} V_1$$

$$= \left[\frac{1}{6} \cdot \frac{15}{5}\right] V_2 - 2V_1$$

$$= \frac{V_2}{2} - 2V_1$$

**6. Attempt any two parts of the following :**

**(a) (i)** Add and subtract without converting the following two octal numbers 7461 and 3465.

$$
\begin{array}{cc}
7461 & 7461 \\
+3465 & -3465 \\
\hline
13146 & 3774 \\
\hline
\end{array}
$$

**Ans.**

**(ii)** Convert the following numbers as indicated :

(A) $(62.7)_8 = (.............)_{16}$

(B) $(BC\,64)_{16} = (...........)_{10}$

(C) $(111011)_2 = (............)_5$

**Ans. (A)** $(62.7)_8 B = 0.0\overline{11}\ \overline{0010}\ .\overline{1110} = (32.E)_{16}$

**(B)** $(BC\,64)_{16}$

$= 11 \times 16^3 + 12 \times 16^2 + 6 \times 16^1 + 4 \times 16^0$

$= 45056 + 3072 + 96 + 4 = (48228)_{10}$

**(C)** $(111011)_2 = 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0$

$= 32 + 16 + 8 + 0 + 2 + 1 = (59)_{10}$

$$
\begin{array}{r}
0 \to 2 \\
5\,\overline{)2} \to 1 \\
5\,\overline{)11} \to 4 \\
5\,\overline{)59} \\
\end{array}
$$

$= (214)_5$

**(b) (i)** Represent the unsigned decimal number 965 and 672 in BCD and then show the steps necessary to form their sum.

**Ans.** 965

$965 \to \overline{1001}\ \overline{0110}\ \overline{0101}$

$672 \to 0110\ 0111\ 0010$

$\overline{\qquad\qquad\qquad\qquad}$

$\qquad 1111\ 1101\ 0111$

$\qquad +1$

$\qquad +0110\ \ 0110$

$\overline{\qquad\qquad\qquad\qquad\qquad}$

$0001\ 0110\ 0011\ 0111$

$\ \ 1\quad\ \ 6\quad\ \ 3\quad\ \ 7$

**(ii)** Express the Boolean function $F = xy + z$ in a product of max term form.

**Ans.** $F = xy + z$

1st step $f^1 = \overline{xy + z} = (\overline{xy})(\overline{z})$

$= (\overline{x} + \overline{y})(\overline{z})$

$= \overline{x}\,\overline{z} + \overline{y}\,\overline{z}$

2nd step $= \left(\overline{\overline{x}\,\overline{z} + \overline{y}\,\overline{z}}\right)$

$= \left(\overline{\overline{x}\,\overline{z}}\right)\left(\overline{\overline{y}\,\overline{z}}\right)$

$POS = (x+z)(y+z)$

$(x+z+y\,\bar{y})(x\bar{x}+y+z)$

$(x+z+y)(x+\bar{y}+z)(x+y+z)(\bar{x}+y+z) = (x+y+z)(x+\bar{y}+z)(\bar{x}+y+z)$

$f = \pi M(0, 2, 4)$

**(c)** Given the Boolean function.

$F(A, B, C, D) = \bar{A}\,\bar{B}\,\bar{C} + A\bar{C}\,\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$

**(i)** Express it in sum of minterms

**Ans. (i)** $\bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C = \bar{A}\bar{B}\bar{C} + (D+\bar{D})A\bar{C}\bar{D}(B+\bar{B}) + A\bar{B}(C+\bar{C})(D+\bar{D})$

$+ ABC\bar{D} + \bar{A}\bar{B}C(D+\bar{D})$

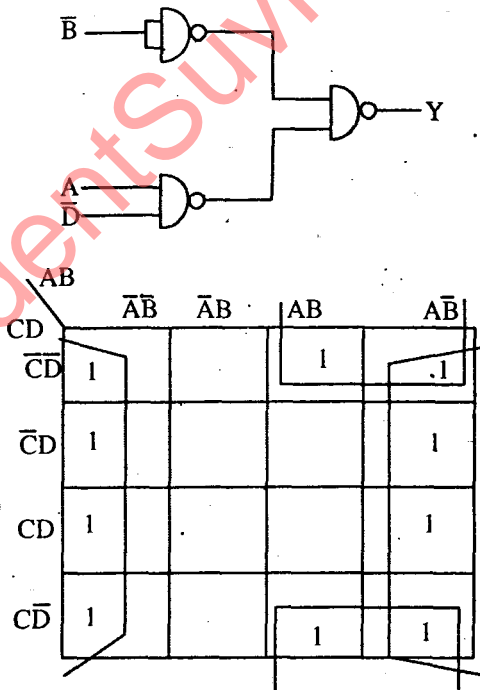$= A\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + ABC\bar{D} + \bar{A}\bar{B}CD$

$= A\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + A\bar{B}C\bar{D} + A\bar{B}C\bar{D} + ABC\bar{D} + \bar{A}\bar{B}CD$

$f(A,B,C,D) = \Sigma m(0, 1, 2, 3, 8, 9, 10, 11, 12, 14)$

**(ii)** Find the minimal sum of products expression using K-map and implement the output using NAND gates only.

**Ans.** $f = \bar{B} + A\bar{D}$

7. Attempt any one of the following :

(a) **Draw the Lissajous pattern you expect when the ratio of the frequency of the vertical input to that of the horizontal input is 1 : 2. Explain with the help of a neat diagram, why you get this pattern.**

Ans. $\dfrac{\text{Frequency of vertical input}}{\text{Frequency of horizontal input}} = \dfrac{\text{Horizontal points}}{\text{Vertical points}}$

$$\frac{\text{Frequency of vertical input}}{\text{Frequency of horizontal input}} = \frac{1}{2}$$

A Lissajous pattern is a pattern which is stationary on the screen of a CRO. It means that the spot traces out the same pattern for every cycle of a voltage signal.

In a Lissajous pattern ratio of frequency of vertical signal to the frequency of horizontal signal is equal to the ratio of positive Y peak to positive X peaks.

$$\frac{fy}{fx} = \frac{\text{Positive } y\text{-peaks}}{\text{Positive } x\text{-peaks}}$$

(b) **Explain briefly the working principle of a digital voltmeter. What are the advantages obtained by numeric read out?**
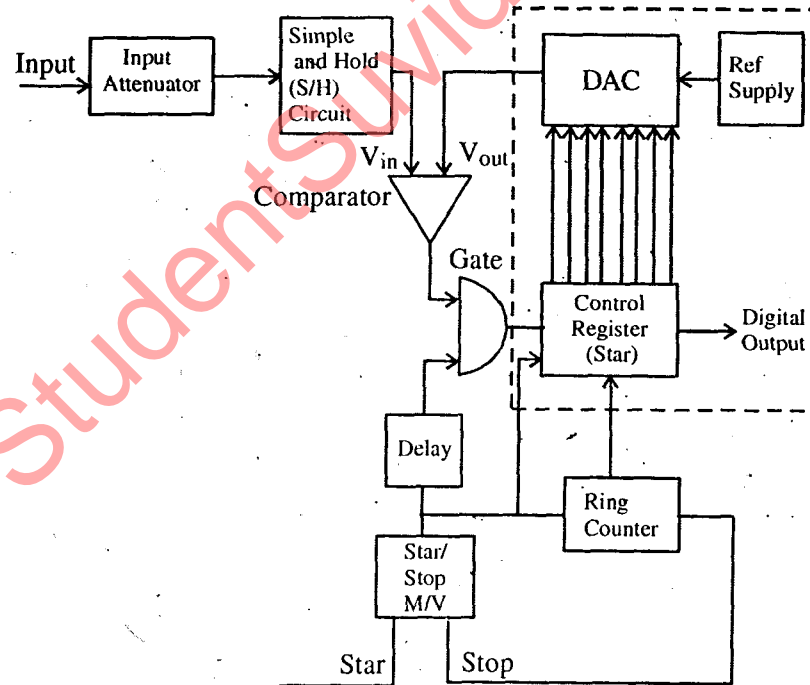
Ans.



**Fig.** Successive Approximation DVM

At the beginning of the measurement cycle, a start pulse is applied to the start-stop multivibrator. This sets a 1 in the MSB of the control register and a 0 in all bits (assuming an 8-bit control) its reading would be 10000000. This initial setting of the register causes the output of the D/A converter to be half the reference voltage, i.e., 1/2 V. This converter output is compared to the unknown input by the comparator. If the input voltage is greater than the converter reference voltage, the comparator output produces an output that *causes the control register to retain the 1 setting in its MSB and the converter continues to supply its* reference output voltage of 1/2 $V_{ref}$.

The ring counter then advances one count, shifting a 1 in the second MSB of the control register and its reading becomes 11000000. This causes the D/A converter to increase its reference output by 1 increment to 1/4 V. i.e., 1/2V + 1/4 V, and again it is compared with the unknown input. If in this case the total reference voltage exceeds the unknown voltage, the comparator produces an output that causes the control resister to reset its second MSB to 0. The converter output then returns to its previous value of 1/2V and awaits another input from the SAR. When the ring counter advances by 1, the third MSB is set to 1 and the converter output rises by the next increment of 1/2V +1/8V. The measurement cycle thus proceeds through a series of successive approximations. Finally, when the ring counter reaches its final count, the measurement cycle stops and the digital output of the control register represents the final approximation of the unknown input voltage.