B.TECH. EEC-101

FIRST SEMESTER EXAMINATION, 2009-2010

ELECTRONICS ENGINEERING

Time : 3 *Hours* *Total Marks :* 100

Note : *Attempt all questions.*

SECTION-A

1. Attempt all parts of this question. All parts of this question carry equal marks. This question contains TEN objective/Fill in the blank type/True False type questions: **2×10=20**

(i) When PN-junction is biased in the forward direction ..... in each region are injected into the other region.

Ans. Mojority change carriers

(ii) In a centre-tap full-wave rectifier, V_m is the peak voltage between the centre-tap and one end of the secondary. The PIV of the nonconducting diode is ..... when the filter is not connected.

Ans. 2Vm

(iii) Which of the following statement is best suited for a Zener diode ?

(a) It is rectifier diode.

(b) It works in the forward bias region.

(c) It is a constant voltage device.

(d) It is mostly used in clipping circuit.

Ans. (c) It is a constant voltage device.

(iv) An ordinary transistor is called 'bipolar junction transistor' because it has two poles: one positive and other negative. (True/ False)

Ans. False

(v) A common emitter transistor amplifier has a gain of 150. The output voltage is measured as 2 V AC, the input voltage will be .....

Ans. gain $\frac{V_{output}}{V_{input}}$

$$\Rightarrow 150 = \frac{2V}{V_i} \Rightarrow V_i = \frac{2}{150} = .0133V$$

(vi) The operation of a JFET involves :

(a) A flow of minority carriers.

(b) A flow of majority carriers.

(c) Recombination.

(d) Negative resistance.

Ans. (b) A flow of majority carriers.

(vii) An ideal operational amplifier is used to make an inverting amplifier. There are two input terminals of the operational amplifier and are at the same potential because :

(a) The two inputs are directly short circuited internally.

(b) The input resistance of the operational amplifier is infinity.

(c) The open loop gain of the operational amplifier is infinity.

(d) All the above except option (a).

Ans. (d) All the above except option (a).

(viii) The α and β of a transistor are 0.99 and 99 respectively. If its I_{CBO} is 0.1 A, then its I_{CEO} will be .....

Ans. $ICEO = \frac{I_{CBO}}{1-\alpha} \Rightarrow I_{CEO} = \frac{0.1}{1-.99} = 10A$

(ix) A basic meter can be converted into an ohmmeter by connecting :

(a) a variable in series.

(b) a battery in series.

(c) Both (a) and (b)

(d) None of the obove

Ans. (c)

(x) (i) A + A′ B =

(ii) A . (A′+ B) =

Ans. (i) A + A′ B = (A + A′) (A + B) = A + B

(ii) A(A′ + B) = A.A′ + A.B = A.B

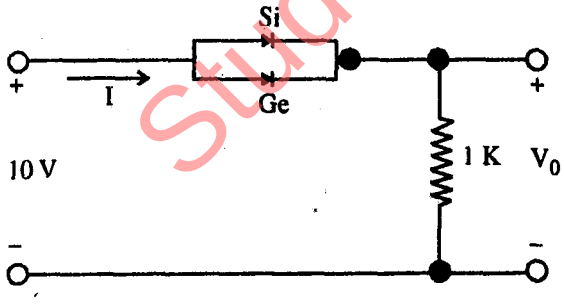
SECTION - B

2. Attempt any three parts of this question. All parts of this question carry equal marks : 10×3=30

(a) (i) Differentiate between static and dynamic resistance of diode.

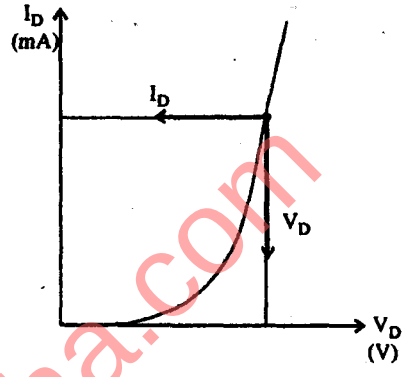
(ii) Explain the two break down mechanisms of a reverse bias diode.

(iii) Determine V_0 and I for the following circuit.



Ans. (i) **Static Resistance :** The application of a dc voltage to a circuit containing a semiconductor diode will result in operating point on the characteristic curve that will no change with time. The resistance of the diode at this operating time is called static resistance.

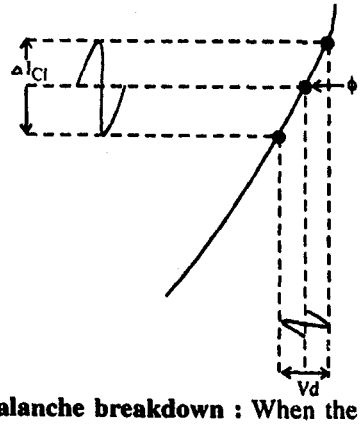
$$R_D = \frac{V_D}{I_D}$$



Dynamic resistance : The static resistance of the diode is independent of the shape of the characteristic.The dynamic resistance depend on the input applied. The varying input will move the operating point up and down.

$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

It defines a change in voltage and current.

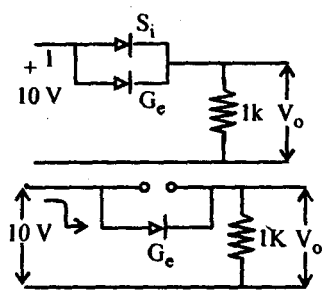


(ii) **Avalanche breakdown :** When the voltage occurs the diode increases in the reverse bias region, the velocity of the minority carriers responsible for the reverse saturation current

will also increase. Then velocity and KE will be sufficient to release additional carriers through collisions. This is an ionization process and these carriers will help the process where high avalanche current is established and the proces is avalanche process.

Zener breakdown : This process occurs when there is strong electric field in the region of the function that can disrupt the bonding forces within the atom and generate carriers. It occurs below 6V.

(iii) For i/p = 10 V, Ge diode will be on due to its low cut in voltage.



Ge = 0.3 V Si = 0.7 V

$10\ V - 0.3\ V - V_0 = 0$

$$\boxed{V_0 = 9.7\ V}$$

$V_0 = I.\ 1K$

$$\boxed{I = \frac{9.7K}{1K} = 9.7mA}$$

(b) (i) Which of the transistor curents is always the largest? Which one is the smallest? Which two are relatively close in magnitude?

(ii) Draw the small signal equivalent circuit of a BJT and explain each component.

Ans. (i) In the transistor there are three currents I_E, I_C and I_B.

$I_E = I_C + I_B$; hence I_E (emitter current) is always the largest due.

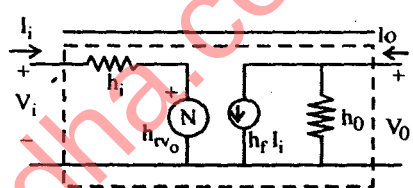
IB current is very small, ssince it is due to the recombination of electron and holes. If the base widlts is widlts is very small, this current is very small or can be neglected. In this case

$I_E = I_E + I_B$

$I_B \approx$ Very Small

$$\boxed{I_E \approx I_C} \quad \left\{\begin{matrix}\text{Emitter} \\ \text{current}\end{matrix} = \begin{matrix}\text{Collector} \\ \text{current}\end{matrix}\right\}$$

(ii) $h_i = \left.\frac{V_i}{I_i}\right|_{V_0 = o}$ $\Rightarrow$ i/p impedance



$h_r = \left.\frac{V_i}{V_o}\right|_{I_i = 0}$ $\Rightarrow$ reverse transfer voltage ratio

$h_f = \left.\frac{I_o}{I_i}\right|_{V_0 = 0}$ $\Rightarrow$ forward transfer current ratio

$h_0 = \left.\frac{I_0}{V_0}\right|_{I_i = 0}$ $\Rightarrow$ Output conductance

(c) Define the following :

1. **Drain to source saturation current of JFET.**
2. **Pinch off voltage of JFET.**
3. **Voltage controlled resistance of JFET.**
4. **Virtual ground in an op-amp.**
5. **Voltage gain of a non-inverting amplifier.**

Ans. 1. I_{DS} : When $V_{GS} = 0$ and V_{DS} = some positive value applied accross the channel. The

gate and source are at same potential. When $V_{DD} = V_{DS}$ is applied the electrons are drawn to the drain terminal, estabilishing the conventional current I_0. The current stors that the drain avalanche source currents are equivalent, i.e., $I_D = I_S$.

2. **Pinc off voltage :** When V_{DS} is increased from 0 to few volts, the current will increase As V_{DS} increased and approaches a level V_{pi}, the depletion regione will widen, causing reduction in channel width. The reduced path of conductance causes the resistance to increased. If VDS is increase to a level where it appears that the two depletion regions would touch is refered as pinch-off and the level of V_{DS} that establishes this condition is reffered to as pinch off voltage i.e., I_D is pinched off and reduced to OA.

3. **Voltage controlled resistance of JFET :** In this region, the JFET resistance is controlled by the device between drain and source function $V_{DS} < V_P$ are a function of applied voltage V_{GS}. As V_{GS} becomes more and more negative the slope of each curve becomes more and more horizontal, coresponding to an increasing resistance level.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

4. **Virtual Ground :** o/p voltage is limited by the supply voltage of few volts, voltage gain is very high, e.g., $V_0 = -10V, A_V = 20000$

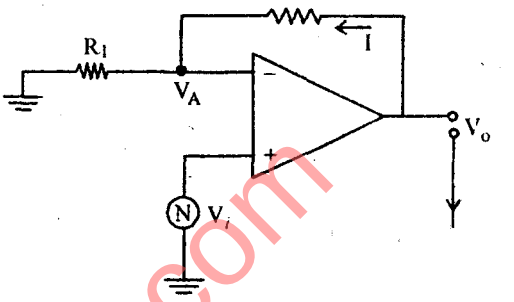
$$V_i = \frac{-V_0}{A_V} = \frac{10}{20000} = 0.5 \text{ mV}.$$

i.e., V_i is very small and may be considered 0 V. This V_i is not exactly 0 V, leads to the concept that at the amplifier i/p there exists a vertical short circuit or virtual ground. The virtual ground implies that although the voltage is nearly 0 V, there is no current through the amplifier i/p to ground.

5. **Voltage gain of non-inverting amp :**

Applying KCL

$$\frac{V_0 - V_A}{R_f} = \frac{V_A - 0}{R_1}$$



Now according to vertical ground concept : $V_A = V_i$

$$\frac{V_0 - V_i}{R_f} = \frac{V_i}{R_1} \Rightarrow \frac{V_o}{R_f} = V_i\left[\frac{1}{R_f} + \frac{1}{R_1}\right]$$

$$\Rightarrow V_0 = V_i R_f \left[\frac{R_1 + R_f}{R_f . R_1}\right]$$

$$\Rightarrow \boxed{V_o = V_i^o\left[1 + \frac{R_f}{R_1}\right]} \text{ proved}$$

(d) (i) Prove the following identity :

$(x_1 + x_2) . (x'_1 . x'_3 + x_3) . (x'_2 x_1 . x_3)' = x'_1 . x_2$

Ans. (ii) $(x_1 + x_2)(x'_1 x'_3 + x_3) . (x'_2 x_1 . x_3)' = x'_1 . x_2$

Taking L.H.S,

$\Rightarrow (x_1 + x_2)(x_3 + x'_1)(x'_2 . x_1) + (x_3)'$

$\Rightarrow [x_1 + x_3 + x_1 x'_1 + x_2 x_3 + x'_1 x_2][x_2 + x'_1] + x'_3$

$\Rightarrow (x_1 x_3 + x_2 x_3 + x'_1 x_2)(x'_1 + x_2 + x'_3)$

$\Rightarrow x_1 x'_1 x_3 + x_1 x_2 x_3 + x_1 x_3 x'_3 + x'_1 x_2 x_3 + x_2 x_3 + x_2 x_3 x'_3 + x'_1 x_2 + x'_1 x_2 + x'_1 x_2 + x'_1 x_2 x'_3$

$\Rightarrow x_1 x_2 x_3 + x'_1 x_2 x_3 + x_2 x_3 + x'_1 x_2 + x'_1 x_2 x'_3$

$\Rightarrow x_2 x_3 + x_2 x_3 + x'_1 x_2$

$\Rightarrow x_2 x_3 + x'_1 x_2 \Rightarrow x_2 \left[x_3 + x'_1\right]$

Not proved

(ii) Define :

1. **Canonical form**
2. **Standard form**
3. **Sum of the products**
4. **Product of the sums**
5. **Don't care terms.**

Ans. 1. Canonical form : A boolean function formed by each combination of the variables giving I/O in the function are called canonical SOP form Y = AB + $\bar{A}$B. or canonical POS form y = (A + B) ($\bar{A}$ + B).

2. **Standard form :** A boolean function expressed with terms that may contain one, two or any number of literal is standard form. e.g., SOP form Y = AB + $\bar{A}$ ϕOS form Y = (A + B) ($\bar{A}$).

3. **SOP form :** It is the sum of product form. It can be standard canonical form. Std SOP form may not contain all the literals from which function is formed whereas in canonical SOP all the literals are present in each product term.

   Simple SOP Y (A,B,C) = AB + AC Canonical Y(A, B, C) = ABC + $\bar{A}$BC

4. **POS form :** It is the product of sum form. It is again two types normal/standard POS, Y(A, B, C) = (A + B)–(A + C) and second canonical POS Y(A, B, C) = (A + B + C). ($\bar{A}$ + $\bar{B}$ + $\bar{C}$)

5. **Don't care terms :** When some of the min terms / max terms in the boolean function or in the truth table do not appear or their values are of no consequence, these minterms/ maxterms are called don't care terms.

(e) Explain, how do we measure the voltage, current and the phase of a waveform using the CRO ?

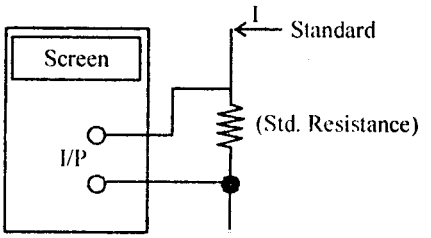
Ans. MMT of voltage using CRO :

- Note down the selection in volts / division from the front panel, selected for measurement.
- Adjust shift control to adjust signal on screen so that it becomes easy to count no. of divisions coresponding to peak to peak value of signal.

$$V_{p-p} \text{ no. of division or units stored} \times \left(\frac{\text{Volts}}{\text{divisions}}\right)$$

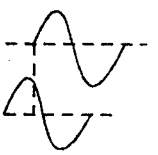
MMT of current :

- The CRO is basically voltage indicating device to measure the current, a known standard resistance is taken and current is passed though it. The voltage a cross resistance is displayed on CKO. This measured voltage is divided by standard resistance to give unknown current value.



Phase Mmt :

- To measure the phase of waveform, two signals of known frequency are applied to two deflection plates.



- The no. of divisions are counted between the two w/fs by which they are separated. The time period of both the w/fs are same are counted. The phase difference is counted since for complete 1 cycle the phase is 360°.

$$\text{Phase difference} = \frac{\text{Measured phase} \times \text{Time period}}{360°}$$

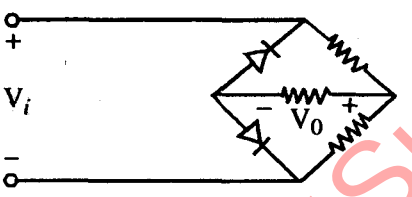
SECTION - C

Note : *Attempt all questions.* (10 × 5 = 50)

All questions carry equal marks.

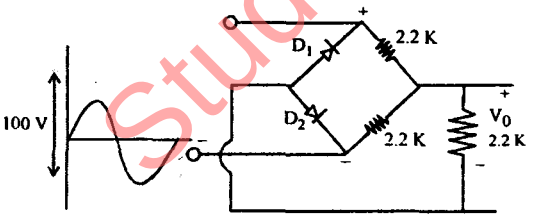
3. Attempt any two parts of the following :

(a) Sketch v_0 for the following circuit and determine the dc value of output voltage. Input to the circuit is 100 V peak to peak sine wave :



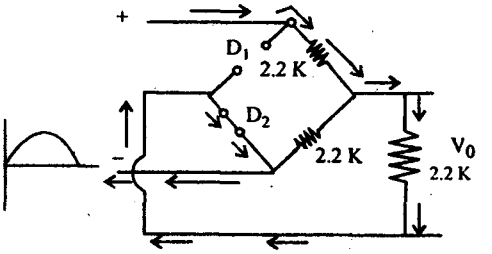
Diodes are ideal. All resistances are 2.2 kΩ

Ans. D_1 & D_2 are ideal. It is a full wave rectifier.



I_n Positive half cycle :

D_1 = RB D_2 = F.B, the direction of current is as shown by bold lines.



V_o = B + Ve half of V_i

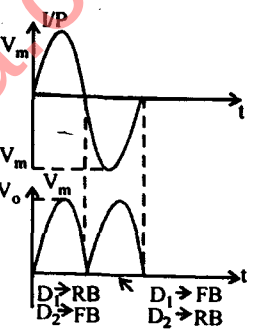
= V_m (Diodes are ideal)

In (negative) half cycle :

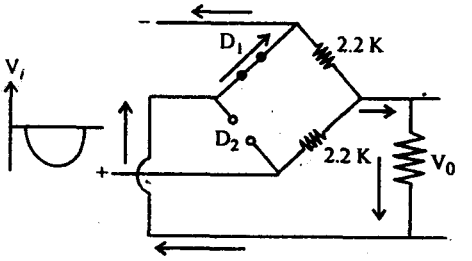
D_1 = D_2 = RB the circuit

D_1 → short circuit

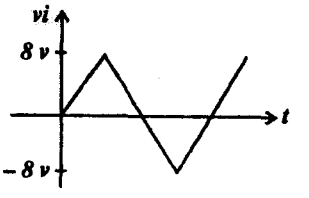
D_2 → Open circuit

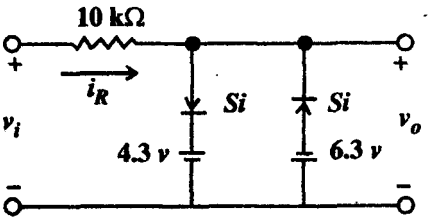


$V_o = V_m$



(b) Sketch i_R and v_0 for the following circuit :

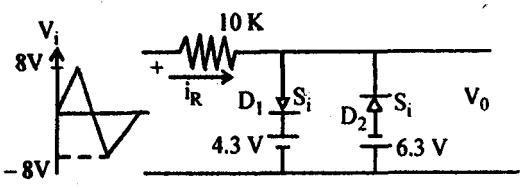




Ans. I_n +ve half cycle :

for $V_i = 0.7V + 4.3V$

$= 5V$



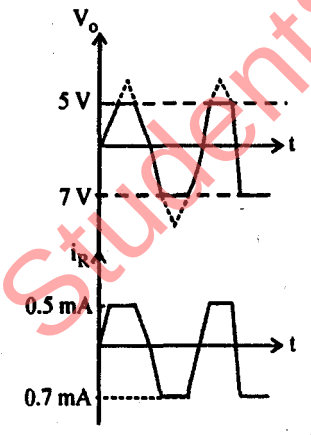
$V_i < 5$ V, $D_1 \rightarrow$ R.B

$D_2 \rightarrow$ R.B

$V_o = V_i$

$Vi > 5V$ $D_1 \rightarrow$ F.B

$D_2 \rightarrow$ R.B



$V_o = 5V$

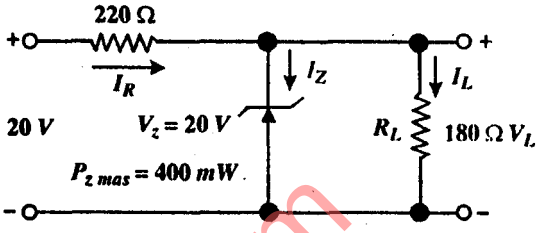
For –ve half cycle

For $V_i = -0.7V - 6.3\ V = -7\ V$

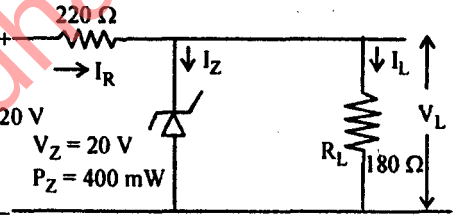
$V_i > -7\ V$ D_1 & D_2 R.B. $V_o = V_i$

$V_i < -7\ V$ $D_1 = R.B$ $D_2 =$ F.B $V_o = -7\ V$

(c) Determine V_L, I_L, I_Z and I_R for the following circuit.



Ans. Determining the state of zener diode by removing it from the network. Let 'V' be the voltage accross zener diode.



$$V = V_L = \frac{R_L - V_i}{R + R_L} = \frac{180 \times 20\,V}{220 + 180} = \frac{3600}{400} = 9V$$

Since $V < V_Z$, the diode is off and open circuit equivalance is substituted .i.e.,

$$\boxed{V_L = V = 9V}$$

$$V_R = V_i - V_L = 20\,V - 9V = 11V$$

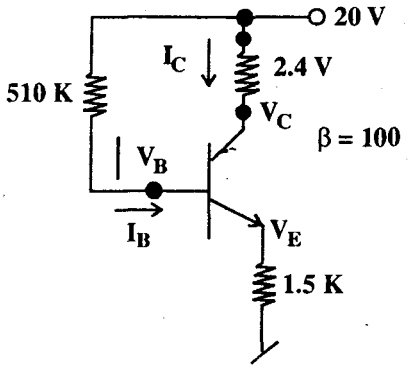
$$\boxed{I_Z = 0\ A}$$

$$\boxed{I_L = \frac{9\,V}{180\,\Omega} = .05\,A}$$

$$\boxed{I_R = I_L = .05A} \text{ or } \boxed{I_R = \frac{11V}{220\ \Omega} = .05}$$

4. Attempt any one of the following :

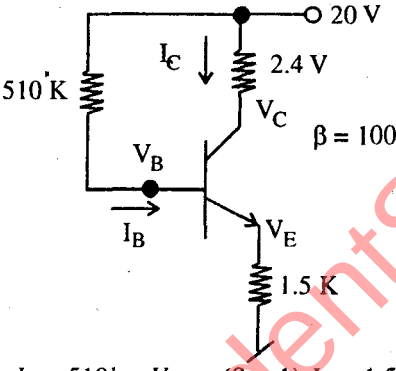
(a) Determine I_C, V_E, V_B, V_C and I_B for the following circuit



Ans. Applying KVL in Base-emitter side :

$20\ V - I_B \times 510\ K - V_{BE} - I_E \times 1.5\ K = 0$

$I_E = (\beta + 1) I_B$



$20\ V - I_B \times 510k - V_{BF} - (\beta + 1)\ I_B \times 1.5\ x = 0$

$$I_B = \frac{V_{CC} - V_{BF}}{R_B + (1+\beta) R_E}$$

$$I_B = \frac{20V - 0.7V}{510 + (1+100)1.5}$$

$= .029$ mA

Applying KVL in Collector emitter loop

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$I_E \approx I_C$

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 0$

$= 20\ V - 2.9\ (2.4 + 1.5)$

$= 8.69\ V$

$V_E = I_E - R_E \qquad I_E \approx I_C = 2.9\ mA$

$= 2.9 \times 1.5$

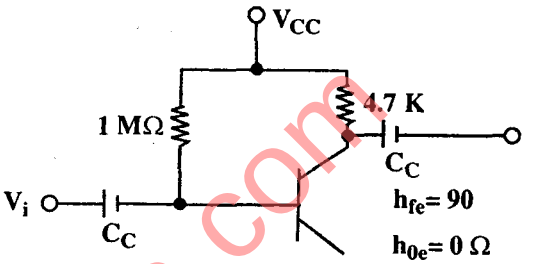
$= 4.35\ V$

$V_{CE} = V_C - V_E \Rightarrow V_C = V_{CE} + V_E$

$= 0.7 + 4.35\ V$

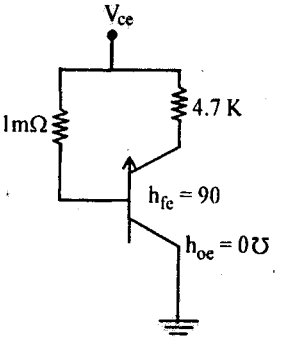
$= 5.05\ V$

(b) Determine V_{CC} for the folowing circuit it the voltage gain A_V = -200.



Ans. $A_V = -200\ (\beta = h_{fe} = 90)$

$$A_V = \frac{-R_C}{r_e} \qquad \left(r_o = \frac{1}{h_{oe}} = \infty\right)$$



$$-200 = -\frac{4.7K}{r.e} \Rightarrow r_e = \frac{4.7K}{200}$$

$= 23.5\ \Omega$

$$r_e = \frac{26mV}{I_E} \Rightarrow I_E = \frac{26mV}{23.5} = 1.106\ mA$$

$$I_E = (\beta+1) I_B \Rightarrow I_B = \frac{I_E}{\beta+1} = \frac{1.106}{90+1} = .012mA$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \Rightarrow I_B R_B + V_{BE} = V_{CC}$$

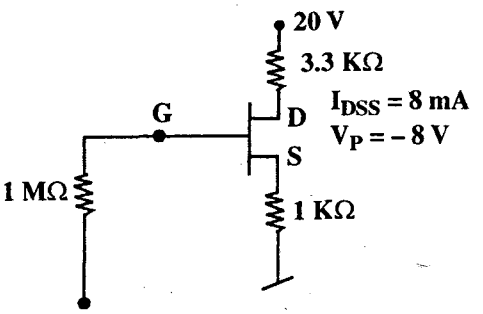
$$\Rightarrow V_{CC} = .012 \times 10^{-3} \times 1 \times 10^6 + 0.7$$

$$= .02 \times 10^3 + 0.7$$

$$V_{CC} = 12.7 \text{ V.}$$

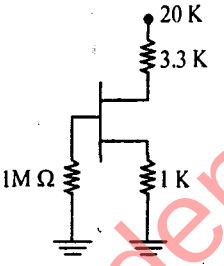
5. Attempt any one of the following :

(a) Determine V_{GS}, I_D, V_{DS}, V_D, V_G, and V_S for the following circuit :



Ans. $I_{DSS} = 8$ mA

$V_P = -6$ V.



$$V_{GS} = -I_D R_S$$

$$= -I_D \times 1 \times 10^3$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

$$= 8\text{mA}\left(1 + \frac{I_D \times 1 \times 10^3}{-6}\right)^2$$

$$I_D = 8 \text{ mA}\left[1 + \left(\frac{I_D \times 10^3}{6}\right)^2 - 2\frac{I_D \times 10^3}{6}\right]$$

$$= 8\text{mA}\left[1 + \frac{I_D^2 \times 10^6}{36} - \frac{2I_D \times 10^3}{6}\right]$$

$$36\, I_D = 8 \text{ mA } (36 + I_D^2 \times 10^6 - 2I_D \times 10^3)$$

$$36\, I_D = 8 \times 10^{-3} [36 + I_D^2 \times 10^6 - 2\, I_D \times 10^3]$$

$$4.5 \times 10^3\, I_D = 36 + I_D^2 \times 10^6 - 2\, I_D \times 10^3$$

$$I_D^2 \times 10^6 - 6.5 \times 10^3\, I_D + 36 = 0$$

Solving the equation.

$I_D = 2.6$ mA

$V_{GS} = -2.6$ V

$V_{DS} = V_{DD} - I_D (R_S + R_D)$

$= 20 - 2.6$ (1K + 3.3 K)

$= 8.82$ V

$V_S = I_D R_S$

$= 2.6 \times 1$ K $= 2.6$ V

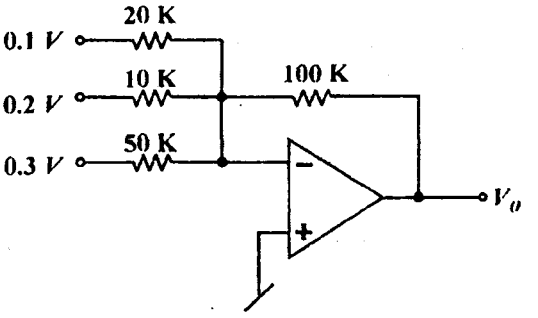
$V_G = 0$V

$V_D = V_{DS} + V_S = 8.82 + 2.6$ V $= 11.42$ V

(b) (i) Enlist the characteristics of an ideal operational amplifier (op-amp).

(ii) Draw the circuit of a subtractor using op-amp and explain its working.

(iii) Determine the V_0 for the following circuit :



Ans. (i) Characteristics of ideal of amp :

(i) I/p resistance $= \infty\ \Omega$

(ii) o/p resistance $= 0\ \Omega$

(iii) Gain $= \infty$

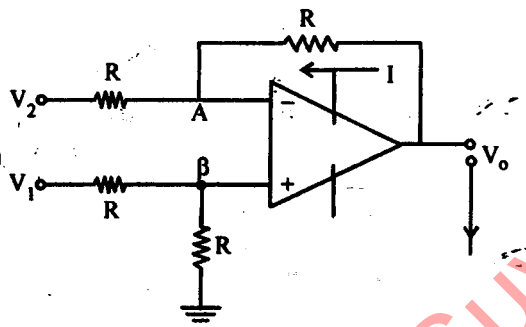
(iv) B.W $= \infty$

(v) Offset voltage $= 0$

(vi) CMRR $= \infty$

(vii) Slow rate $= \infty$

(ii) Subtractor using o/p amp : Let all the resistances are equal = R



Using superposition theorem, finding V_0 for i/p V_1 and V_2 is grounded

$$V_B = \frac{V_1 \times R}{R+R} = \frac{V_1}{2}$$

$$V_A = V_B = \frac{V_1}{2}$$

Since it will work as non-inverting amplitude

$$V_{01} = \left(1+\frac{R}{R}\right).V_i = V_1 \qquad \text{....(i)}$$

Calculating V_{o2} when V_1 = grounded it will work like inverting amplitude

$$V_{o2} = -\frac{R}{R}.V_2$$

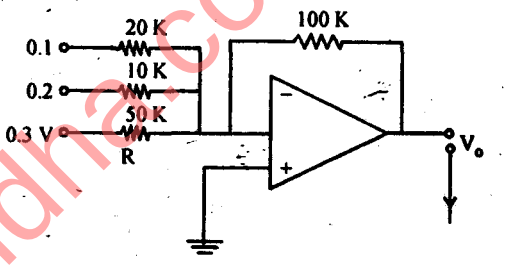
$$= -V_2$$

Adding both the outputs.

$$V_o = V_{o1} + V_{o2}$$

$$\boxed{V_o = V_1 - V_2}$$

(iii) $V_o = -\left[\frac{R_{fV_1}}{R_1} + \frac{R_{fV_2}}{R_2} + \frac{R_{fV_3}}{R_3}\right]$



$$= -\left[\frac{100}{20}\times 0.1 + \frac{100}{10}\times 0.2 + \frac{100}{50}\times 0.3\right]$$

$$= \left[5 \times 0.1 + 10 \times 0.2 + 2 \times 0.3\right]$$

$$= -\left[0.5 + 2 + 0.6\right]$$

$$= -3.1\ \text{V}$$

6. Attempt any two of the following :

(a) Convert the following numbers :

$(2CCD)_{16} = (\ )_8 = (\ )_5$

$(7841)_9 = (\ )_{10} = (\ )_4 = (\ )_2$

Ans. $(2CCD)_{16} = (26315)_8$

$= (331334)_5$

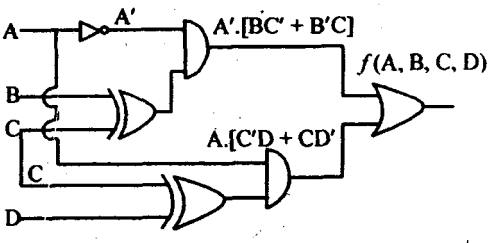
$(7841)_9 = (5788)_{10} = (1122130)_4$

$= (1011010011100)_2$

(b) Realize the following experssion using Ex-OR/Ex-NOR gates and basic gates if required $f(A, B, C, D) = A'BC' + AC'D + ACD'$

Ans. $f(A, B, C, D) = A'BC' + A'B'C + AC'D + ACD'$

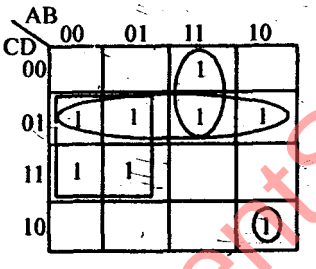
$= A'[BC' + B'C] + A[C'D + CD']$



(c) Minimize the give function using K-map and convert the minimized function into POS form

$f(A, B, C, D) = \Sigma (1, 3, 5, 7, 9, 10, 12, 13)$

Ans.



$f = \bar{C}D + \bar{A}D + AB\bar{C} + A\bar{B}C\bar{D}$

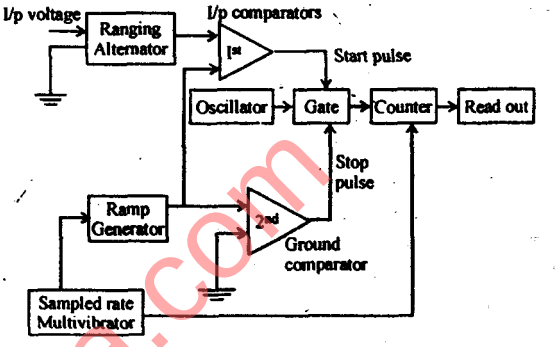
Function in POS form :

$$f = \left[(C+\bar{D}).(A+\bar{D}).(\bar{A}+\bar{B}+C).(\bar{A}+B+\bar{C}+D)\right]$$

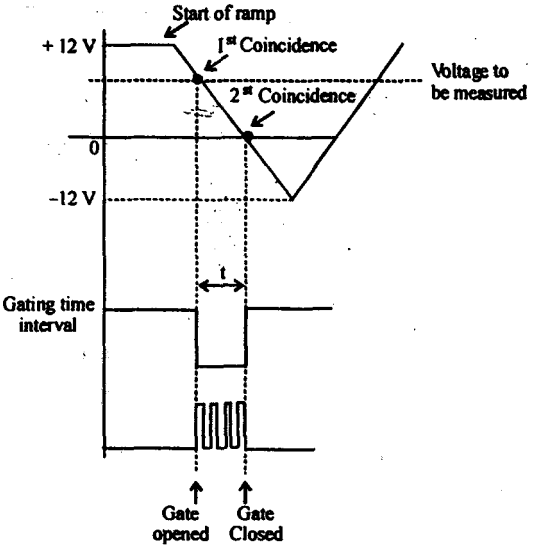
7. Attempt any one part of the following:

(a) Explain the working of digital voltmeter with help of a block diagram.

Ans. Digital voltmeter : At the start of mmt, a ramp voltage is initiated which is compared with o/p voltage. When these two voltages are same the comparator generates a pulse which opens a gate i.e., the i/p comparator generates a start pulse. The ramp continues to decrease and finally reaches 'o' value. This is sensed by 2nd comparator to counter i.e., ground comparator. At ''0V, this comparator produces a stop pulse which closes the gate. The no. of clock pulses

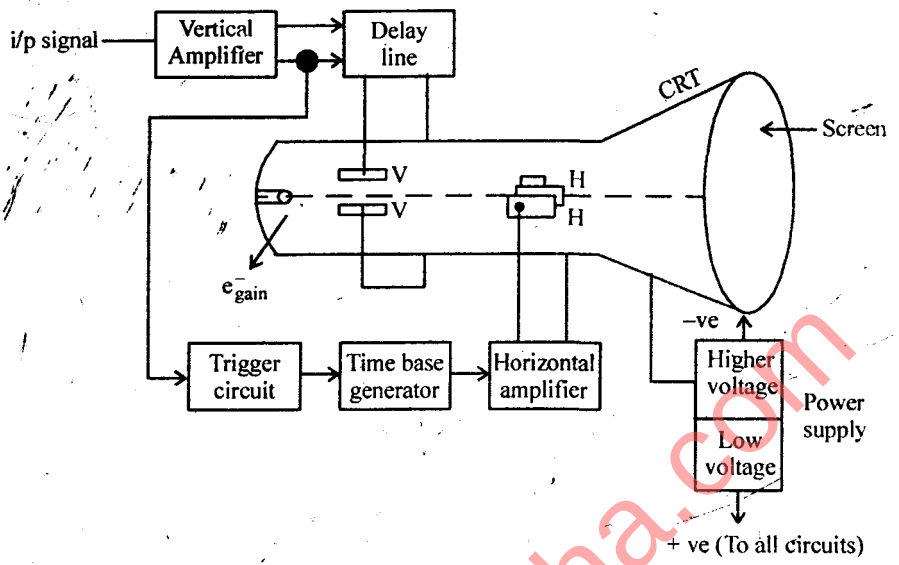


are measured by the counter. Thus the time duration for which the gate is opened is proportional to the i/p voltage. The magnitude of count indicates the magnitude of the i/p voltage displayed by read out display



(b) Explain the working of CRO with the help of a block diagram.

Ans.



CRT : It is used to emit the e^{-1}s required to strike the phosphor screen to produce the spot for the visual display of signal.

Vertical amplifier : The i/p signals are generally not strong to provide measurable deflection on the screen, thus this stage is used to amplify the i/p signals. It contains attenuator also.

Delay line : It is used to delay the signal for some time in vertical section. When the delay line is not used, some part of signal gets lost.

Trigger circuit : To synchronize horigontal deflection with vertical deflection, synchronize or triggering circuit used.

Time Base Generator : It is used to generate the sawtooth voltage required to reflect the beam in horizontal section.

Horizontal amplifier : The strength of sawtooth voltage is not strong enough, so it is passed though this amplifier before gets applied to horizontal plates.

Power supply : It provides voltage required by CRT to generate and accelerate an e^- beam and voltages required by other circuits of oscilloscope.