Roll No.
Total No. of Pages : 2
Total No. of Questions : 09

# B.Tech (CSE/IT) (Sem.-3) <br> DIGITAL CIRCUITS \& LOGIC DESIGN <br> Subject Code : CS-205 <br> Paper ID : [A0453] 

Time : 3 Hrs.
Max. Marks : 60

## INSTRUCTION TO CANDIDATES :

1. SECTION-A is COMPULSORY.
2. Attempt any FOUR questions from SECTION-B.
3. Attempt any TWO questions from SECTION-C.

SECTION-A ( $10 \times 2=20$ Marks $)$

1. Write short notes on :
(a) Convert $\left(\begin{array}{llllllll}1 & 0 & 1 & 1 & 0 & 1 & 1 & 1\end{array}\right)_{2}$ to decimal equivalent.
(b) Convert the following BCD number to its decimal equivalent. 10011000.01000101
(c) Realize NAND gate with the help of NOR gates only.
(d) What are the advantages of CMOS memory chips over bipolar memory chips?
(e) What is multiplexer? Explain with the help of an example.
(f) How sequential circuits are different from the combinational circuits?
(g) What is the function of multivibrator?
(h) What is resolution in $\mathrm{A} / \mathrm{D}$ converter?
(i) What is shift register?
(j) Why do we use PGAs?

## SECTION-B

$(4 \times 5=20$ Marks $)$
2. Minimize the following Boolean expression.
$\mathrm{Y}=(\overline{\mathrm{AB}} \mathrm{C}+\mathrm{A} \overline{\mathrm{BC}})(\overline{\mathrm{A}} \overline{\mathrm{B}} \mathrm{C}+\mathrm{A} \overline{\mathrm{B}} \overline{\mathrm{C}})$
3. Design full subtractor using demultiplexer.
4. Design mod-8 down asynchronous counter using T flip-flops.
5. Draw and explain the circuit of TTL NAND gate with open collector.
6. State and prove De-Morgan's theorems.

## SECTION-C

( $2 \times 10=20$ Marks)
7. Write short notes on following :
(a) Successive approximation A to D Conversion Technique
(b) Multivibrators
8. Differentiate between custom and semi-custom VLSI design.
9. What is race-around condition? How it is eliminated in Master-Slave J- K flip-flop?

