Roll No. .....

Total No. of Page : 3

BT-7/D11 : 7817

ECE-401E : VLSI Design

Time : Three Hours

Maximum Marks : 100

Note:- Attempt any FIVE questions by selecting atleast ONE question from each unit.

UNIT - I

Q.1. Describe with illustration, the double-metal P-well CMOS fabrication process. List all the masks involved in the sequence of usage. 20

Q.2 a) Draw VTC of a saturated-loaded MOS inverter and discuss the critical voltages. How does VTC change with increasing $\beta_{drive}/\beta_{load}$. 10

b) Draw the stick diagram of a 1-bit full adder circuit in double metal p-well CMOS process.

UNIT - II

Q.3. a) A MOSFET is fabricated with the following parameters: 10

W = 10 μm, L=6 μm, t_{ox} = 0.08 μm,

$\mu_n = 580 cm^2/Vsec$, $V_{TO} = 1.0$ V, $N_A = 10^{15}$ cm^{-3}. The device is subjected to the constant field scaling with $\alpha = 4$. Calculate the original and scaled values of (i) device transcoductance parameter, β (ii) body bias coefficient, γ.

b) What are layout methodologies? Discuss. 10

Q.4 a) Define R_S, $\square C_g$ and τ. Find the value of sheet resistance of the channel and $\square C_g$ of a transistor in 5μm technology. Also find the value of τ for the technology. Given that $\mu_n = 600$ $cm^2/Vsec$, $C_{ox} = 4 \times 10^{-4}$ $pF/\mu m^2$, $V_T = 1.0$ volt, gate voltage w.r.t. source = 3 volts. 10

b) What is Packaging? What are the various types of packages and issues involved? 10

UNIT - III

Q.5 What do you understand by routing? Disucss the various routing algorithms. What is the grid model for global routing? 20

Q.6 Discuss the various Partitioning Algorithms. Discuss the advantages and disadvantages of each. 20

UNIT - IV

Q.7 Describe the delay models in Physical Design. How are timing constraints applied? 20

Q.8 Write short notes on:

a) Performance issues in circuits 10

b) Timing driven placement 10