B.E.
Fifth Semester Examination, May-2008
Microprocessor & Interfacing (EE-309-E)

Note : Attempt any five questions. All questions carry equal marks.

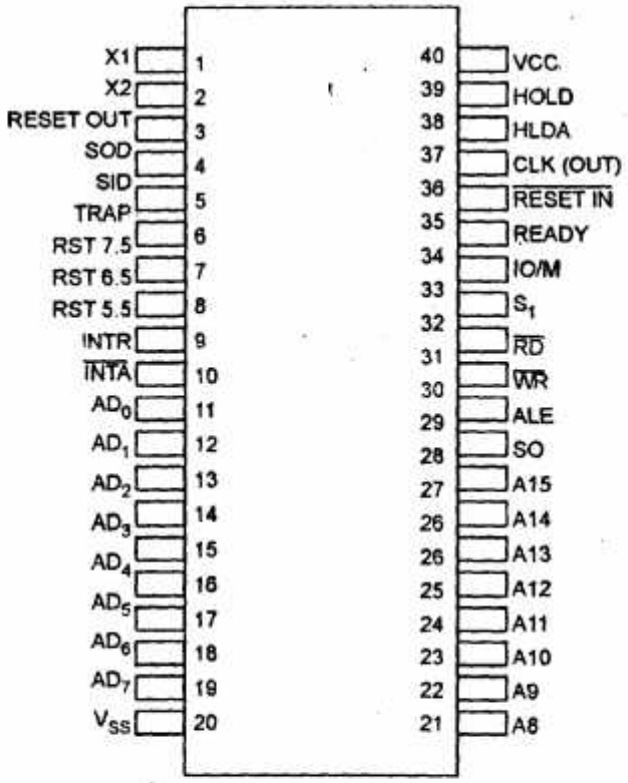
Q. 1. (a) Give and explain pin diagram of 8085. **15**

Ans. The term microprocessor unit (MPU) is similar to the term central processing unit (CPU) used in traditional computers.

8085 microprocessor can almost qualify as an MPU, but with following two limitations :

(i) The low order address bus of the 8085 microprocessor is multiplexed (time shared) with the data bus. The buses need to be multiplexed.

8085 Microprocessor Pinout Signals :



8085 Pinout

(ii) Appropriate control signals need to be generated to interface memory and I/O with the 8085.

8085 Interrupts and Externally Initiated Signals :

INTR (Input)	:	Interrupt request
	:	Used as a general purpose interrupt
INTA (Output)	:	Interrupt Acknowledge

	:	Used to acknowledge an interrupt
RST 7.5 (Input)	:	
RST 6.5	:	Restart Interrupts
RST 5.5	:	7.5, 6.5, 5.5 – priority order.
TRAP (Input)	:	Non-maskable interrupts
	:	Highest priority
HOLD (Input)	:	Indicates that a peripheral such as DMA (Direct-Memory Access) controller is requesting the use of address and data buses.
HLDA (Output)	:	Hold acknowledge
READY (Input)	:	Signal is used to delay the microprocessor.

Power Supply and Clock Frequency :

V_{CC} = + 5 power supply.

V_{SS} = Ground Reference.

X_1, X_2 : A crystal is connected at these two pins.

CLK (OUT) : Clock output.

8085 Machine Cycle Status and Control Signals :

Machine Cycle	IO/$\overline{M}$	S_1	S_2	Control Signals
Opcode fetch	0	1	1	$\overline{RD}$ = 0
Memory Read	0	1	0	$\overline{RD}$ = 0
Memory Write	0	0	1	$\overline{WR}$ = 0
I/O Read	1	1	0	$\overline{RD}$ = 0
I/O Write	1	0	1	$\overline{WR}$ = 0
Interrupt acknowledge	1	1	1	INTA = 0
Halt	Z	0	0	
Hold	Z	x	x	$\overline{RD}$, $\overline{WR}$ = Z
Reset	Z	x	x	$\overline{INTA}$ = 1

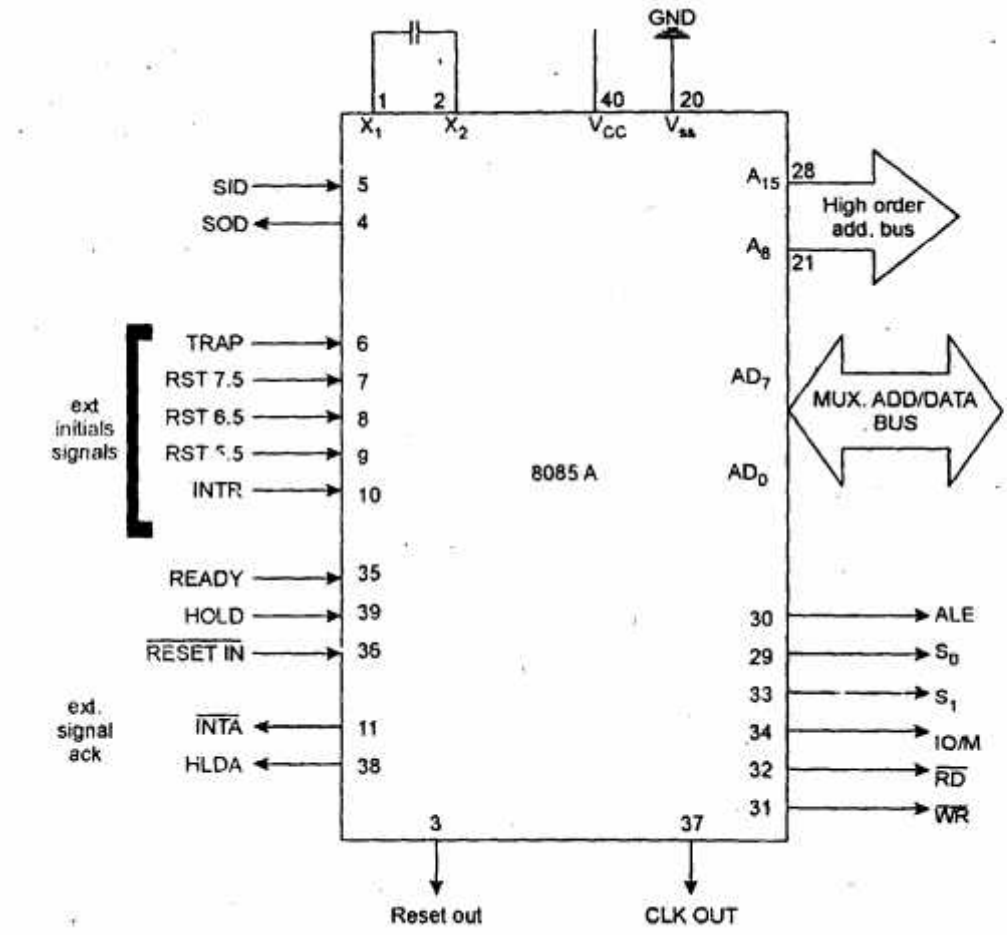
Q. 1. (b) How address/data bus are muitiplexed in 8085 and what is the advantage of multiplexing ?

Ans. Multiplexed Address/Data Bus : The signal lines ($AD_7 - AD_0$) are bidirectional; they serve a dual purpose. They are used as low order address bus as well as data bus.

In executing an instruction, during the earlier part of the cycle, these lines are used as the low order address bus.

During the later part of the cycle, these lines are used as data bus.

However the low order address bus can be separated from these signals by using a latch.



Control & Status Signals

Q. 2. (a) Describe the various interrupts used in 8085 microprocessor. **10**

Ans. 8085 interrupts and externally initiated signals :

INTR (Input) : Interrupt Request
: Used as a general purpose interrupt.

$\overline{\text{INTA}}$ (output) : Interrupt Acknowledge.
: Used to acknowledge an interrupt.

RST 7.5 (Inputs) : Restart interrupts

RST 6.5 : These are vectored interrupts that transfer the program control to specific memory location. They have higher priorities than INTR interrupts.

TRAP (Input) : Non-maskable interrupt
: has highest priority.

HOLD (Input) : This signal indicates that a peripheral such as DMA (Direct memory access) controller is requesting the use of address and data buses.

HLDA (Output) : Hold acknowledge.

READY (Input) : Used to delay the microprocessor, Read or write cycles until a slow-responding peripheral is ready to send/data.

Q. 2. (b) Explain the following instructions of 8085 : **10**

(i) LDA,

(ii) DADB,

(iii) XCHG,

(iv) EI,

(v) STAXD.

Ans. (i) LDA : 16 bit

- Load accumulator direct
- 3 byte instruction.
- Copies the data byte from the memory location specified by the 16 bit address in the second and third byte.
- The second byte is a line number
- The third byte is a page number
- The addressing mode is direct.

(b) DADB

(c) XCHG

(d) EE

(e) STAXD

(ii) DADB : Add Register pair to H & L Register

Opcode	Operand	Bytes	M-Cycles	T-states	Hex Code
DAD	Reg-pair	1	3	10	B 09

If the result is larger than 16 bits, C4 flag is set.

No other flags are affected.

(iii) XCHG : Exchange H and L with D and E

Opcode	Operand	Bytes	M-Cycles	T-states	Hex Code
XCHG	None	1	1	4	FB

The contents of Reg. H are exchanged with the contents of D and Reg. L are exchanged with Reg E. No flags are affected.

(iv) EI : Enable interrupt

Opcode	Operand	Bytes	M-cycles	T-states	Hex code
E1	None	1	1	4	FB.

Description : The interrupt enable flip-flop is set and all interrupts are enabled. No flags are affected.

(v) STAXD : Store accumulator direct

Opcode	Operand	Bytes	Meycles	T-states	Hex Code
STAX	D Reg	1	2	7	0 12

- No flags affected
- Contents of accumulator are copied into the memory location specified by the contents of the operand. Contents of the accumulator are not altered.

Q. 3. (a) Give various addressing modes of 8085. **14**

Ans. ADDRESS BUS : The 8085 has 8 signal lines $A_{15} - A_8$, which are unconditional and used as the high order address bus.

Multiplexed Address/Data Bus : The signal lines $AD_7 - AD_0$ are bidirectional; they serve a dual purpose they are used as the low order address bus as well as data bus.

In executing an instruction, during the earlier part of the cycle, these lines are used as the low order address bus.

During the later, part of the cycle, these lines are used as low order address bus. During latch this is also known as multiplexing the bus.

However the low order address bus can be separated from these signals by using a latch.

Q. 3. (b) Obtain physical address of data byte in a segment having segment address of $(1234)_{16}$ and on offset addresss of $(0022)_{16}$.

Ans. Segment address $= (1234)_{16}$

Offset address $= (0022)_{16}$

Physical address $= 16 \bullet \text{Segment address} + \text{Offset address}$

$= 16 \bullet (1234)_{16} + (0022)_{16}$

$= (12340)_{16} + (0022)_{16}$

$= 12340$

$= \dfrac{0022}{12362}$

$= 12362$ H Ans.

Q. 4. (a) Give & explain architecture of 8086. **12**

Ans. The 8086 central processing unit is divided into two independent functional units.

They are :

(i) Bus interface unit (BIU)

(ii) Execution unit (EU)

Bus Interface Unit : It is responsible for transfer of instructions, addresses and data on the system bus to the execution unit.

Functional parts are :

(i) Instructional queue (IO)

(ii) Segment Register (SR)

(iii) Instruction Pointer (IP)

Execution Unit : Works in parallel with BIU. The phases of execution of the instruction are Fetch, Decode, Execute, and write

Functional parts of EU are :

(i) Control System & Instruction Decode

(ii) Arithmetic and Logic Unit (ALU)

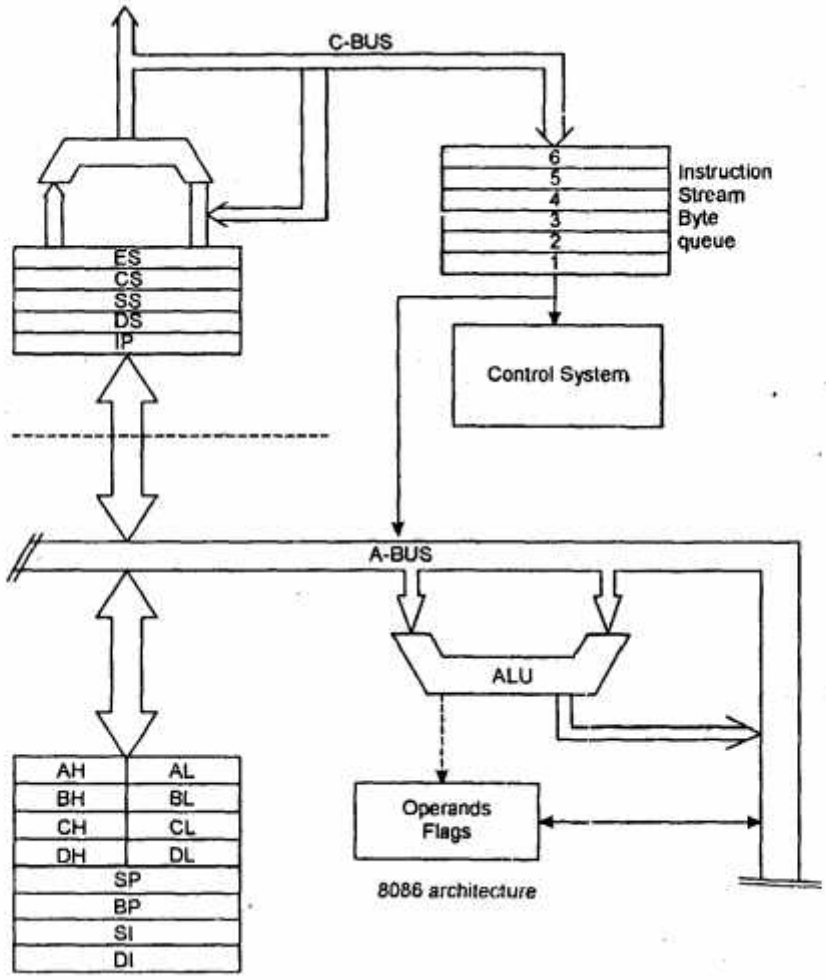
(iii) Flag Register

(iv) General Purpose Register

(v) Stack Pointer Register.

(vi) Pointer and Index Register

Instruction Set of 8086 : The processor 8086 supports a variety of instructions to perform the movement of data (between memory, CPU and I/O devices), arithmetic and logical operations, branch and control of processor operations, string operations and protection control.



8086 architecture

8086 Instructions are classified as :

(a) Data transfer instructions

(b) Arithmetic and logical instructions

(c) Branch Instructions

(d) Processor control Instructions

(e) String Operation Instructions

(f) Protection Control Instructions

Q. 4. (b) Explain the concept of memory segmentation and program relocation in 8086. **8**

Ans. Memory Segmentation : The 8086 processor allows the programmer to specify four distinct segments for simultaneous use within a program. They are code segment, data segment, stack segment. and extra segment. Such segment is 64 kb in size and hence the program can reference only 250 kb in the memory at any instance of time.

The code segment contains the instructions of a program, the data segment contains the program data; the extra segment may be used for storing the additional data and to hold and manipulate the string data; the stack segment may be used for dedicated purpose of string the program's run time stack.

Program Reallocation : The processor requires 2 memory cycles to access a word from odd address of the memory location :

For example :

```
MOV : BX, 0001
MOV : AX, [BX]
```

It reads the contents of the word at memory location 0001H into the register AX and places contents of the memory location 0001H in the register AL and 0002H in register AH. First it reads a word from memory location 0000H and then reads a word from memory location 0002H. Hence is known as program relocation.

Q. 5. Write an assembly language program in :

(i) 8085 to find largest number from an array of 10 elements. **10**

Ans. 8085 to find largest number from an array of 10 elements.

Program : Mneumonics

```
IN FIH
MOV B, A
IN F2H
ANI SOH

MOV C, A
MOV A, B
ANI 50H

ANA C
JN2 SHTDWN
MOV A, B
```

```
ANI IFH
OUT F3H
JMP START

MVI A, 40H
OUT F3H
HLT
```

Q. 5. (ii) Write an assembly language program in 8086 to reverse a string. **10**

Ans.

```
_ main proc _ far
assume cs: _ TEXT, ds: _ DATA
push das
XOR ax, ax
push ax
mov ax, se g_DATA
mov  ds ay
Mov  ah, 40h
Mov  bx, stdout
Mov cx,  msg_len
Mov dx offset  msg.
int 2lH
ret
_Main endp
_TEXT ends
end _main
```

Q. 6. (a) Give PIN diagram of 8255. **10**

Ans. Pin Names :

$D_7 - D_O$	:	Bidirectional data bus.
RESET	:	Reset input
$\overline{CS}$	:	Chip select
$\overline{RD}$	:	Read input
$\overline{WR}$	:	Write input
A_0, A_1	:	Port address
$PB_0 - PB_7$	:	Port B (bit)
$PA_0 - PA_7$	:	Port A (bit)
$PC_0 - PC_7$	:	Port C (bit)
Vcc	:	+5 volts
GND	:	0 volts

Q. 6. (b) Give various modes of 8255.

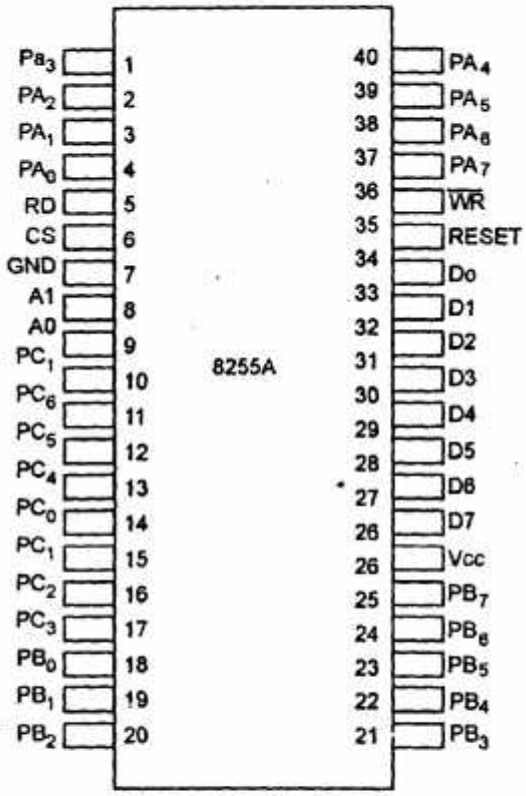
Ans. There are three modes of 8255 :

Mode 0

Mode 1

Mode 2

Pin Configuration



Mode 0 (Simple Input or output)

Here :

- Outputs are latched
- Inputs are not latched
- Ports do not have handshake or interrupt capability.

Mode 1 : Input or Output with Handshake.

Features :

(i) Two ports (A and B) function as 8 bit input/output parts. They can be configured either as input or output ports.

(ii) Each port uses three lines from port C handshake signals. The remaining two lines of port C can be used for simple input/output functions.

(iii) Input and output data are latched.

(iv) Interrupt logic is supported.

Mode 2 : Bidirectional Data Transfer :

This mode is used primarily in applications such as data transfer between two computers or floppy disk controller interface.

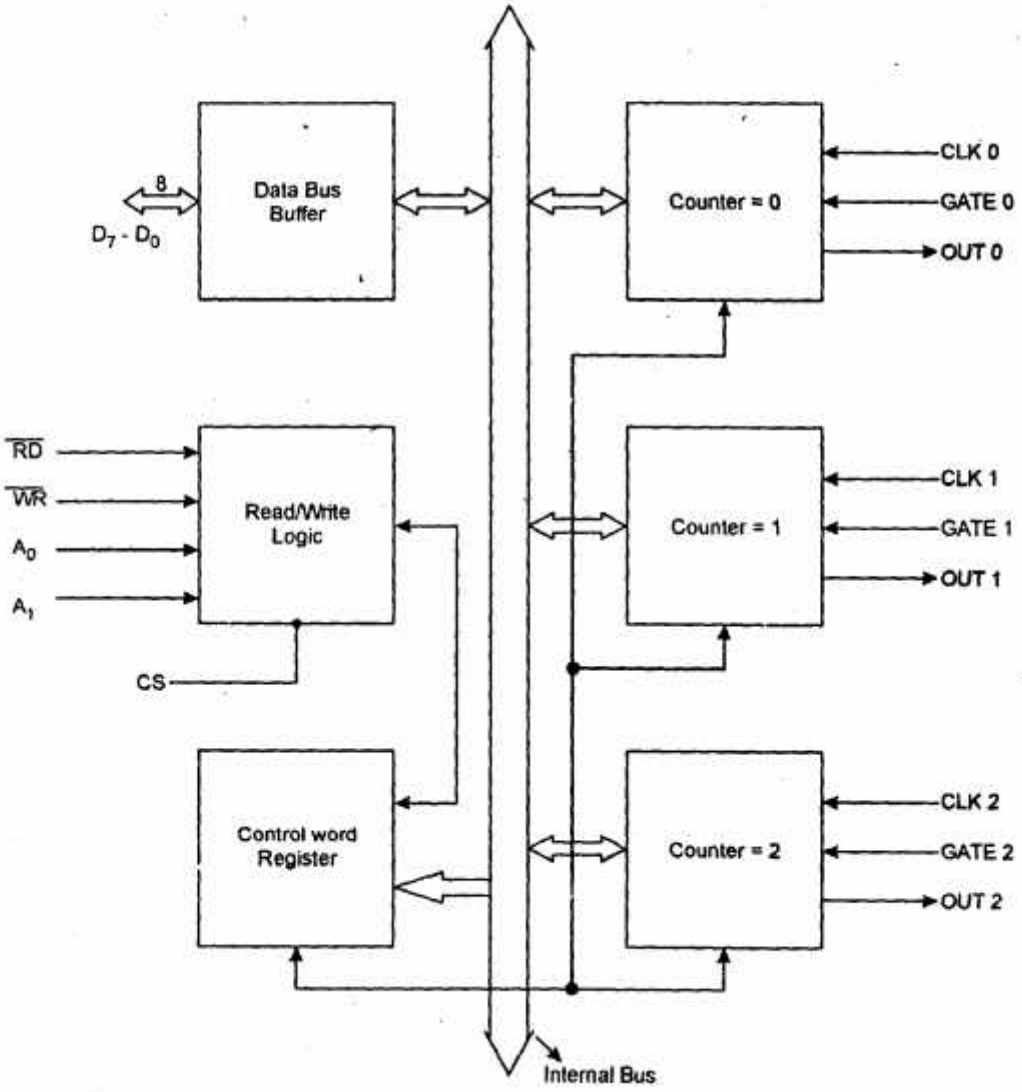
In this mode, port A can be configured as the bidirectional port and port B either in mode 0 or mode 1.

Port A uses 5 signals from port C as handshake signals for data transfer. The remaining three signals from port C can be used as either simple input/output or as handshake for port B.

Q. 7. (a) Give & explain block diagram of 8254. **10**

Ans. Figure shows the block diagram of 8254; it includes three counters (0, 1 and 2) a data bus buffer, read, write control logic and a control register.

Black Diagram



Each counter has two input signals : clock (CLK) and GATE and the output signal OUT.

Data Bus Buffer : This tri-state 8 bit bidirectional buffer, is connected to the data bus of the MPV.

Control Logic : The control section has five signals, $\overline{RD}$ (Read), $\overline{WR}$ (write), $\overline{CS}$ (chip select) and the address lines A_0 and A_1. In a peripheral input/output mode, the $\overline{RD}$ and $\overline{WR}$ signals are connected t· $\overline{IOR}$ and $\overline{IOVW}$, respectively.

In memory mapped input/output these are connected to $\overline{MEMR}$ (Memory Read) and $\overline{MEMW}$ (Memory write).

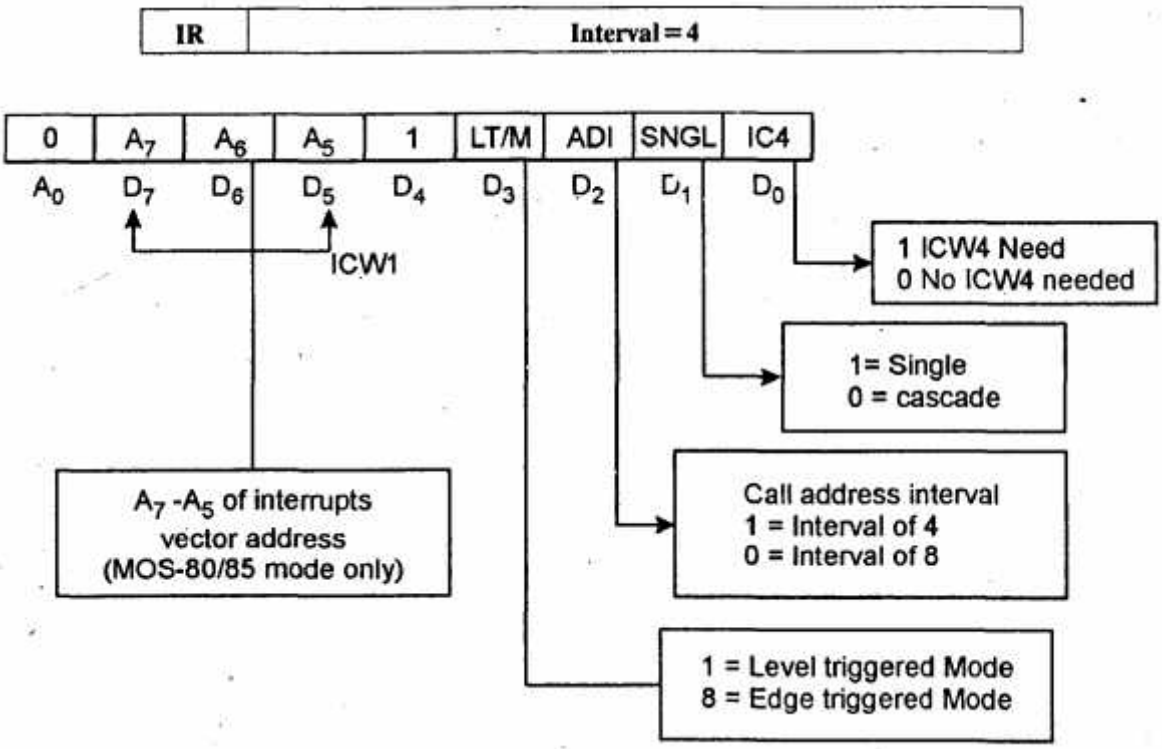
Address lines A_0 and A_1 of the MPU are usually connected to lines A_0 and A_1 of the 8254, and $\overline{CS}$ is tied to a decoded address.

The control word register and counters are selected according to the signals on lines A_0 and A_1

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

Q. 7. (b) Give initialization command words and operational command words of 8259 programmable interrupt controller. **10**

Ans.



	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	A_5	1	1	1	0	0
6	A_7	A_6	A_5	1	6	0	0	0
5	A_7	A_6	A_5	1	0	1	0	0
4	A_7	A_6	A_5	1	0	0	0	0
3	A_7	A_6	A_5	0	1	1	0	0
2	A_7	A_6	A_5	0	1	0	0	0
1	A_7	A_6	A_5	0	0	1	0	0
0	A_7	A_6	A_5	0	0	0	0	0

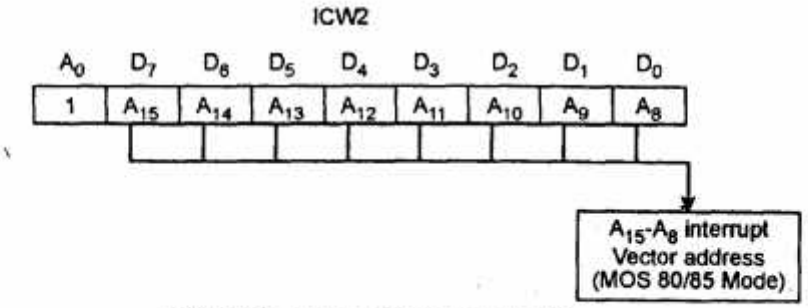
IR	Interval = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	A_7	A_6	A_5	1	1	0	0	0
6	A_7	A_6	A_5	1	0	0	0	0
5	A_7	A_6	A_5	0	1	0	0	0
4	A_7	A_6	A_5	0	0	0	0	0
3	A_7	A_6	A_5	1	1	0	0	0
2	A_7	A_6	A_5	1	0	0	0	0
1	A_7	A_6	A_5	0	1	0	0	0
0	A_7	A_6	A_5	0	0	0	0	0

Q. 8. Write short notes on (any two) : **10, 10**

(i) 8237 DMA controller

(ii) Directives and operators

(iii) PIN diagram of 8254



Initialization comm and works for 8259 A

Ans. (i) 8237 DMA Controller : Direct memory access in an input technique commonly used for high speed data transfer; for example, data transfer between system memory and a floppy disk.

In status check Input/Output and Interrupt Input/Output data transfer is relatively slow because each instruction needs to be fetched and executed.

DMA introduces two new signals available on 8085 HOLD and HLDA (HOLD acknowldege).

HOLD : This is an active high input signal to 8085 from another master requesting the use of the address and data buses.

HLDA : (Hold acknowledge)

This is an active high output signal indicating that the MPV is relinquishing control of the buses.

To perform this function, the DMA controller should have

(a) An data bus

(b) An address bus

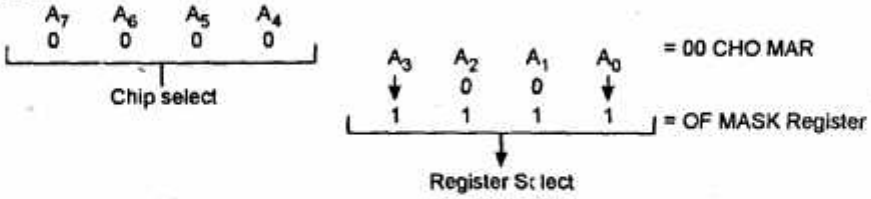
(c) Read/write control signals

(d) Control signals to disable its role as a peripheral and to enable its role as a processor.

This process is called switching from slave mode to the master mode.

DREQ0-DREQ3-DMA Request : These are four independent, asynchronous, input signals to the DMA channels from peripherals, such as floppy disks and the hard disk. To obtain DMA serivce, a request is generated by activating OREQ line of the channel.

Reg Adds.



00 CH_0 Mem. add. Reg.

01 CH_0 Count Reg.

02 CH_1 Mem. add. Reg.

03 CH_1 Count Reg.

04 CH_2 Mem. add Reg.

05 CH_2 Count Reg.

06 CH_3 Mem. add. Reg.

07 CH_3 Count Reg.

08 R/W Status/Command Reg.

09 W/R Request Reg.

0A W/R Single mask Reg.

0B W/R Mode Reg.

0C W/R Clear Byte pointer R/F

0D R/W Master clear /Temp Reg.

0E W/R Clear Mask Reg.

0F W/R All Mask Reg. Bus

8237A DMA controller with Internal Register.

(c) Pin Diagram of 8254 **10,10**

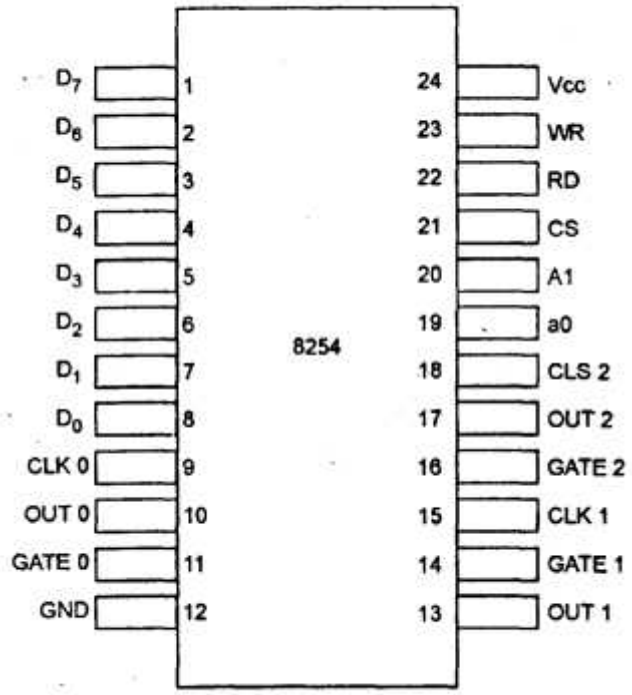
8254 includes three counters 0, 1 and 2, a data bus buffer, Read/write control logic, and a control register, each counter has two input signals-clock (CLK) and GATE : and one output signals OUT.

Data Bus Buffer : This tri-state, 8 bit, bidirectional buffer is connected to the data bus of MPU.

Control Logic : The control section has 5 signals, $\overline{RD}$, $\overline{WR}$, ES, and address lines A_0 and A_1

In the peripheral input/output mode, the $\overline{RD}$ and $\overline{WR}$ signals are connected to $\overline{IOR}$ and $\overline{IOW}$ respectively.

A_1	A_0	Section
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Counter Register



Pin diagram of 8254