B. Tech. 4th Semester (AEIE) F Scheme Examination, May–2014

DIGITAL ELECTRONICS

Paper–EE–204–F

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *Attempt five questions.* ***Question 1*** *is* ***compulsory*** *and one question from each of four sections.*

1. What is a logic gate ? Explain each logic gate :

(a) With truth table and its logic symbol.

(b) Implement the following logic gates using multiplexers

(i) AND gate

(ii) OR gate

(c) Explain Ring Counter

(d) Design the circuit of Half adder using ROM .

5×4

Section–A

2. Minimize the following function using G-M method

(a) $Y = \Sigma m\,(0, 1, 3, 7, 10, 14)$

(b) Convert the following :

(i) $(268.75)_{10}$ to binary, octal and hexadecimal

(ii) $(1100101011.1110)_2$ to octal

(iii) $(360)_8$ to hexadecimal

(c) Minimize the following expression using K-map

(i) $Y = \sum m\ (4, 5, 10, 15)$

(ii) $Y = \pi M\ (3, 6, 9, 14, 15)$

(d) Explain the procedure form generation matrix in binary cycle codes. 5×4

3. (a) Write in detail about various error detecting and correction codes 15

(b) Find 9's complement and 10's complement of following numbers 5

(i) 25

(ii) 155

(iii) 333

(iv) 982

Section–B

4. (a) Design the circuit of full adder using 8:1 multiplexer.

(b) Design a full subtractor using half subtractors. 10,10

5. Give truth table and logic diagram of

(a) 3:8 decoder

(b) Implement the function F (A, B, C) = Σ (1, 3, 5, 6) using decoder

(c) Design a binary to Gray code convertor. 5,5,10

Section–C

6. (a) Give excitation table for following Flip Flops

(i) D Flip Flop

(ii) J K Flip Flop

(iii) T Flip Flop

(iv) SR Flip Flop 5×4

(b) Design 0, 1, 2, 3, 0 counter using D Flip Flop

(c) Explain the working of Master-slave J-K Flip Flop

(d) Explain the working of Serial in Serial out shift register.

7. Design synchronous decade counter using : 10,10

(a) J-K Flip Flops

(b) Give the difference between following

(i) decoder and demultiplexer

(ii) Ripple counter and Synchronous counter

(iii) Latch and Flip Flop.

Section–D

8. (i) Design the circuit of half subtractor using PLA

(ii) Design BCD to Excess-3 code convertor using PLA 10,10

9. (a) Realize the following functions using ROM

(i) $F = \sum m\ (0, 1, 2, 3)$

(ii) $F = \sum m\ (0, 2, 5)$

(b) With the help of state table and state diagram, design a MOD-4 UP/DOWN Counter. 10,10