B.E./B.Tech. 4th Semester (AEIE) E-Scheme

Examination, May–2014

DIGTAL ELECTRONICS

Paper–EE-204-E

Time allowed : 3 hours]. *[Maximum marks : 100*

Note : *Attempt any five questions. All questions carry equal marks.*

1. (a) Convert the following :

(i) $(1101.01101)_2 = (?)_{16}$

(ii) $(3FA\ 7)_{16} = (?)_8$

(iii) $(32.43)_{10} = (?)_8$

(iv) $(100.11)_2 = (?)_{10}$

(iv) $(8435)_{10} = (?)_{16}$ 10

(b) Prove the following :

(i) $AB + ABC + ABCD + ABCDE + ABCDEF = AB$

(ii) $(A + \overline{B} + \overline{C})(A + \overline{B}C) = A + \overline{B}C$ 10

2. (a) Describe the following :

(i) BCD Code

(ii) Excess – 3 Code

(iii) ASCII Code 10

(b) Simplify the following functions

(i) $Y = \pi (0, 1, 2, 3, 6, 8, 11, 12, 13, 15)$

(ii) $Y = \pi M (0, 1, 2, 3, 5, 7, 14) + d (6, 9, 11, 12, 13, 15)$ 10

3. (a) Simplify the Boolean function using Quine Mc Cluskey method.

$f (A, B, C, D) = \Sigma m (1, 2, 3, 6, 9, 12, 14, 15)$ 10

(b) Reduce the given equation into POS form and implement using NOR gates

$Y (A, B, C, D, E) = \pi M (2, 3, 5, 7, 11, 13, 15, 19, 21, 24, 25, 30, 31)$. 10

4. (a) Design a 32:1 multiplexer using 8:1 multiplexer. 10

(b) Design a binary to Gray code converter. 10

5. (a) Convert the following :

(i) S-R to T Flip Flop

(ii) J-K to T Flip-Flop. 10

(b) Design MOD - 10 counter using J-K Flip Flop. 10

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6. (a) Discuss the following TTL output circuit configurations.

   (i) Totem-pole output

   (ii) Open collector output 10

   (b) Explain the working of dual slope ADC. 10

7. (a) Explain the working of R-2R D/A converter. 10

   (b) Write short notes on :

   (i) Sample and Hold circuit

   (ii) Resolution

   (iii) Accuracy 10

8. (a) Compare FPGA with CPLD. 8

   (b) Design the circuit of Half adder using PAL and PLA. 12