Roll No. .....

24143

B. Tech 4th Semester (E. E.) Examination – May, 2013

DIGITAL ELECTRONICS

Paper : EE-204-F

Time : Three hours] *[Maximum Marks : 100*

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions. Question No. 1 is *compulsory* and *one* question from each of *four* Section.

1. (a) Realize the following using NOR gate : $5 \times 4 = 20$

(i) OR gate

(ii) AND gate

(b) Give Boolean expression and Truth Table for following :

(i) AND gate

(ii) Half Adder

(iii) Substracter

(iv) 4 : 1 Multiplexer

(c) Differentiate between :

(i) Latch and Flip Flop

(ii) Decoder and demultiplexer

(iii) Ripple and synchronous counter

(d) What are hazards ?

SECTION – A

2. (a) Use K-map to simplify : 10

(i) $F = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,BCD + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,BC\,\overline{D} + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,CD$

(ii) $F = (AC + A\,\overline{C}\,D)\,(AD + AC + BC)$

(b) Write short notes on : 10

(i) Quine MC- Clusky Method

(ii) Error detecting and correcting codes

3. (a) Convert : 10

(i) 212_8 to decimal

(ii) 399_{10} to octal

(iii) -200_{10} to hexadecimal

(iv) 101101.1_2 to decimal

(v) ABH to binary

(b) Get simplified expression of : 10

Y = F (A, B, C, D) = Σm (1, 2, 8, 9, 10, 12, 13, 14) using Quine -MC Qusky method

SECTION – B

4. (a) Design 16 to 1 multiplexer using 4 to 1 multiplexer. 10

(b) Draw bleach diagram, Truth table and Circuit diagram for 1-bit comparator. 10

5. (a) Implement Full adder using two half address. 10

(b) Realize $y = \overline{A}B + \overline{B}\overline{C} + ABC$ using an 8 to 1 multiplexer. Can it be realized with 4 to 1 multiplexer. 10

SECTION – C

6. (a) Design a MOD-10 down counter using J – K Flip-Flop. 10

(b) Convert : 10

(i) J-K Flip – Flop to D Flip Flop

(ii) S-R Flip – Flop to J-K Flip Flop

7. (a) What is a shift register ? Draw circuit diagram for : 10

(i) Serial in/Serial out

(ii) Parallel in/parallel out Shift registers using J – K Flip – Flops

(b) Give excitation tables for : 10

(i) J – K Flip – Flop

(ii) D Flip – Flop

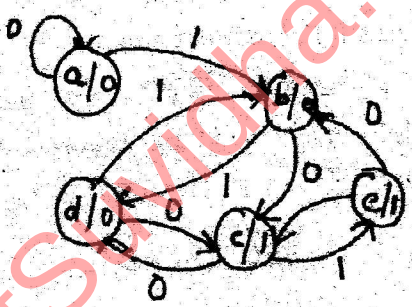
(iii) T Flip – Flop

SECTION – D

8. Reduce state transition diagram of Figure by : 20

(i) Row eliminator method

(ii) Implication Table method



9. Write shorts notes on : 10, 10

(i) ROM and PLA,

(ii) ASM.