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24143

B. Tech. 4th Sem. (E.E/E.E.E/E.C.E./E.I.E./ I.C.E.) (Common to all these Branches) Examination – May, 2011

DIGITAL ELECTRONICS

Paper EE-204-F

Time : Three hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination

Note : Attempt *five* questions. *Q. No. 1 is compulsory* and one questions from each of four Section.

1. (a) Realize the following using Nand Gate :

(i) AND gate,

(ii) EX-OR gate,

(b) Simply :

(i) $F = \overline{A}\,(\overline{B} + \overline{C}) + BC + A\overline{C}$

(ii) $F = \overline{A\,(B + C)} + \overline{A}B + \overline{C}\,\overline{(A + B)}$

(c) Give truth table for :

(i) S-R Flip-Flop,

(ii) J-K Flip Flop.

(d) Differentiate between :

(i) Latch and Flip-Flop,

(ii) Ripple counter and Synchronous counter.

5 × 4

SECTION – A

2. (a) (i) Multiply 4.75_2 by 3.625_2.

(ii) Divide 50_2 by 5_2.

(iii) Convert 2004_{10} to octal

(iv) Convert 7325_8 to binary.

(v) Add $+112_{10}$ and $+65_{10}$ using 2s compliment arithmetic. 10

(b) Use K-map to simplify :

(i) $F = \overline{A}B\overline{C} + A\overline{C}D + BC + \overline{A}\overline{B}D + A\overline{B}CD$

(iii) $F = (AC + A\overline{C}D)(AD + AC + BC)$

3. (a) Write short notes on :

(i) Error detecting and correcting codes,

(ii) Excess-3 code and gray code. 10

(b) Give simplified large equation of Table 1 by Quine-McClusky Method. 10

Table 1

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

SECTION – B

4. (a) Show how 1.6 to 1 multiplexes can be obtained using 4 to 1 multiplexes 10

(b) Draw and explain :

(i) Block diagram,

(ii) Truth Table,

(iii) Circuit for 1-bit comparator. 10

5. (a) Give truth table, Boolean equation and circuit diagram for :

(i) Full Adder,

(ii) Substrater.

(b) What is a demultiplexer. Explain with help of suitable block diagram and logic circuit of 1 to 16 demuliplexer. 10

SECTION – C

6. Design : 20

(i) MOD-8 ripple counter

(ii) Decode synchronous counter using J-K Flip-Flops.

7. (a) What is a shift register. Draw circuit diagram for :

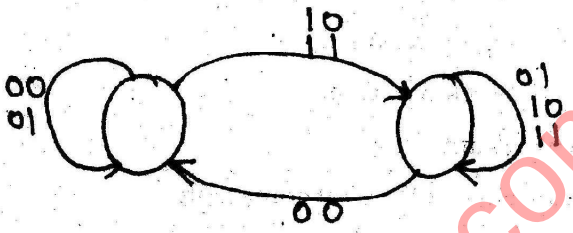
(i) Serial in/parallel out

(ii) Parallel in / serial out shift registers using J-K Flip-Flops. 15

(b) Convert J-K Flip-Flop into D Flip-Flop. 5

SECTION – D

8. (a) Design an asynchronous sequential logic circuit for state transition diagram shown in Figure : 10



(b) Implement a full adder using PLA. 10

9. Write short notes on : 10, 10

(i) RAM and ROM.

(ii) Algorithm State Machine (ASM).