Roll No. .....

2013

B. E. 3rd Semester (I. T.)

Examination – December, 2011

DIGITAL ELECTRONICS

Paper : EE-204-E

Time : Three hours] *[Maximum Marks : 100*

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complain in this regard, will be entertained after examination.

Note : Attempt any *five* questions out of eight questions. All questions carry equal marks.

1. (a) Why NAND and NOR gate are called universal gate ? Explain. 10

(b) Perform the following : 10

(i) Add 52 and 63 in BCD code

(ii) Convert 111011 gray to Binary code

(iii) $(561)_{10} - (443)_{10}$ using 10's complement

(iv) $(98)_{10} - (59)_{10}$ using 9's complement

2. Simplify the following function using Q. M. method. 20

$f(A, B, C, D, E) = \Sigma m\ (1, 2, 3, 6, 8, 9, 14, 17, 24, 25, 26, 27, 30, 31) + \Sigma d\ (4, 5)$ and also verify by k-map.

3. (a) Design 16 : 1 M ∪ X with two 8 : 1 M ∪ X and one 2 : 1 M ∪ X. 10

(b) Design a code converter BCD code to seven-segment display device. 10

4. (a) What do you mean by Race around condition in J. K. FF. How it can be removed ? Explain Master slave FF. 10

(b) Design a synchronous counter using J – K FF which counter 1, 3, 5, 8, 9, 12, 14, 1..... 10

5. (a) Explain the working of Bi-directional shift register. 10

(b) Explain Asynchronous Decade counter. 10

6. (a) Explain R-2R ladder type D/A converter. 10

(b) What do you mean by quantization ? Explain successive approximation A/D converter. 10

7. (a) Compare the advantages and disadvantages of MOS logic over bipolar logic. 10

(b) Explain the :

(i) Interface TTL with CMOS and 10

(ii) CMOS interface with TTL

8. (a) Write short notes on : 10

(i) FPGA

(ii) CPLD's

(b) Implement the full adder using PLA. 10