

Roll No. ....

**2104**

**B. E. (4th Semester) (ECE)**  
**Examination – December, 2011**

**DIGITAL ELECTRONICS**

**Paper : EE-204-E**

***Time : Three hours ]***

***[ Maximum Marks : 100***

*Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.*

**Note :** Attempt any *five* questions out of *eight* questions.

1. (a) Design all Basic and Universal gate using transistor. 10  
(b) Release X-OR gate using 4 NAND gate. 6  
(c) Perform :  
(i) 11001 – 10110  
(ii) 11011 – 11001 using 2's complements. 4
2. (a) The code 101101010 is received. Correct any error. There are four parity bits and add parity is used. 10

(b) Simplify the following : 10

(i)  $\overline{A} \overline{B} \overline{C} + \overline{A} B \overline{C} + A \overline{B} \overline{C} + A B \overline{C}$ ,

(ii)  $\overline{(A+B)} \overline{C} \overline{D} + E + \overline{F}$  and implement with gates.

3. Reduce the following expression using quine - McCluskey method : 20

$Y(A, B, C, D) = \sum m(1, 3, 5, 7, 8, 9, 12, 13, 14, 15)$  and implement using NAND gate only.

4. (a) Why multiplexer is known as a Data selector. Design and explain the  $8 \times 1$  MUX? 10

(b) Design a BCD adder, explain its working. 10

5. (a) Design Mod-10 synchronous counter using J-K Flip Flop. 10

(b) What do you mean by Shift Register? Explain the working of PISO shift register. 10

6. (a) Explain why the outputs of the standard TTL should not be wired together? Under what condition is wiring permissible. 10

(b) Compare the advantages and disadvantages of MOS logic over bipolar logic. 10

7. (a) Explain Dual slope ADC with detail. 10

(b) What is the requirement of converting digital data to analog? Draw and explain weighted register concept for such condition. 10

8. Write short notes on the following :

(a) ROM and PROM,

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(b) PAL and PLA.

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